VLBI 2010 using the RDBE and Mark5C

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VLBI2010 System
RDBE

- Roach Digital BackEnd (RDBE)
- Joint development project Haystack / NRAO
- Goal
  - Standard hardware configuration that can be ordered
    • RDBE-H
  - Standard software interface / command set
  - Common VHDL framework to accommodate
    • multitude of signal processing chains
- Components
  - Hardware
  - FPGA personalities
  - Server software
RDBE-H Block Diagram
(common hardware for NRAO and Haystack)
RDBE-H Firmware

• Personality types (FPGA code)
  – Polyphase filter bank (pfbg) Version 1.4 (Haystack)
    • Input is two 512MHz IFs
    • Output
      – 16 of 32 possible 32-MHz channels on one CX4
      – Mark5B format
  • Synchronous detection from a noise diode for system temperature measurement
• Monitoring
  – Tsys
  – 1pps
RDBE-H Firmware

- Digital down converter (ddc) (NRAO)
  - Input is two 512MHz IFs
  - Output anticipated to be eight tunable channels (two working now)
  - Bandwidths ranges down in binary steps from 64 MHz to 62.5kHz
  - Output is 5008-byte packets in Mark5B format
Mark5C

- Joint development effort of MIT Haystack, NRAO and Conduant Corporation
- Designed to meet the Mark5C specification
  - MIT Haystack Memo #57
  - VLBA Sensitivity Upgrade memo #12
- 4 Gbps recording capability
- Three components
  - Hardware
  - Software development kit (SDK)
  - Application
Mark5C Hardware

• Amazon streamstor controller card
  – Controller card (Mark5B+)

• 10Gbps Ethernet daughter board
  – CX4 physical connector
  – Maximum ingress rate is 4Gbps
  – Receive only device
    • No transmit capability designed into initial release
Mark5C Software

• SDK 9.X
  – Standard function calls
    • To configure, control and monitor
      – Controller Card
      – 10G daughter board
      – Disk modules
    – Supports 32 bit Linux kernels
  – Supports > 1TB disk drives
  – Using SDK 9.1
Mark5C Software

• Applications
  – drs
    • VLBI Data Recording Service
    • Write capabilities
      – 2Gbps bank mode
    • Version 0.9.4
  – fuseMk5
    • Read capability
  – Numerous utilities
    • Updated utilities SSErase, SSReset
    • Command line interface and graphical user interface
VLBI2010 Upgrade
RDBE-Q

• Hardware
  – 2\textsuperscript{nd} iADC card
    • Four 512MHz IFs
  – Modification to ALC to handle 4 IFs
  – Utilize 2 10G CX4 output ports
    • 8 Gbps aggregate
      – 4 Gbps / Ethernet port
RDBE Firmware

• Version 2.0
  – Utilize the polyphase filter bank design
    • Based on version 1.4
    • Process 4 IFs
  – Software settable quantization
  – Output Data
    • Sixty four 32MHz channels
    • Data will be complex
    • VLBI Data Interchange Format (VDIF)
RDBE Firmware

– Output data (cont)
  • 32 channels / thread ID / 10G CX4 port
  • 8884 bytes of VDIF data
– Utilized the VLBI Transport Protocol (VTP)
  • Currently under investigation, but:
    – FPGA resource constraints
      • Version 1.4 utilized 65% for 2 IF design
Mark5C Application

• drs version 0.9.5
  – Adds 4Gbps write capability support
    • Dual bank mode
  – disk2file capability
    • fuseMk5 not required to access data on the disk

• drs version 1.0
  – VDIF
    • Limited timing checking of scans
Contributors

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Thank you / Questions?