The Stability of Delay in VLBI Digital Backends

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Delay (in)stability in VLBI digital backends (DBE)

Most of delay instability in electronic devices is related to temperature variations.

There are 4 options to deal with it in case of DBE:

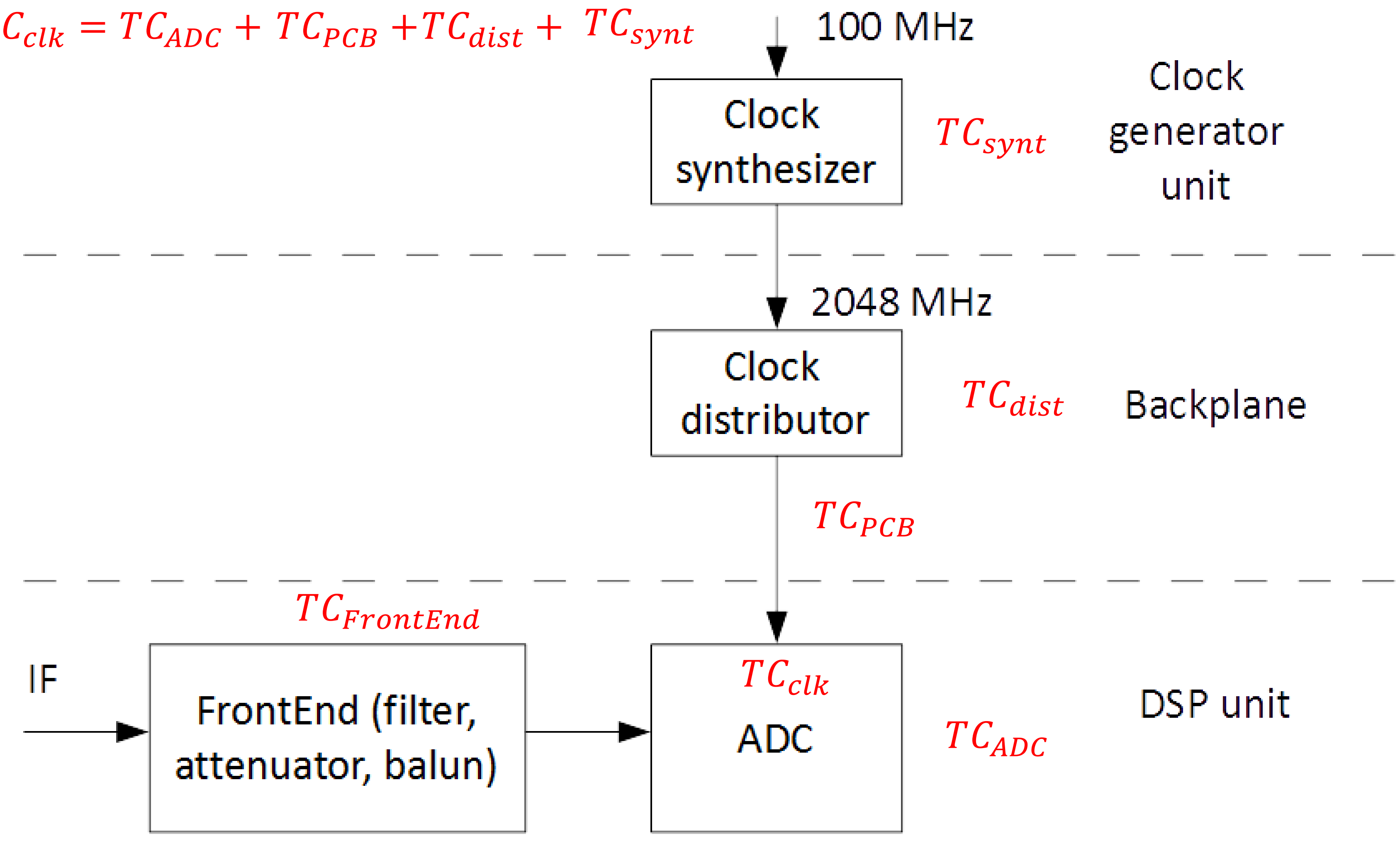
1. Reduce temperature coefficient (TC) of DBE by appropriate design and tuning
   - TC of delay in DBE's parts?
2. Stabilize temperature
   - Appropriate level of temperature variations? => TC of delay in DBE's parts?
3. Calibrate variations by using temperature sensors and known TC and take it into account in correlator
   - TC of delay in DBE's parts?
4. Directly measure delay variations
   - Measurement technique?

Temperature coefficients of delay in DBE
DBE internal delays measurement technique

TC of DBE parts

$$TC_{DBE} = TC_{FrontEnd} - TC_{clk}$$

$$TC_{clk} = TC_{ADC} + TC_{PCB} + TC_{dist} + TC_{synt}$$



Temperature coefficient of delay in ADC analog frontend

Filters

TC depends on fractional bandwidth, sharpness (order), manufacturing technology

For IF filters (1-2 GHz) it is usually < 1 ps/K

Dependence on frequency

Example: MiniCircuits LFCN-1700+ (-3dB @ 2050 MHz) has **TC < 80 fs/K**

Attenuators

Group delay: tens of ps => low TC

Typical TC for 31 dB digital attenuator: about **10 fs/K**

Baluns

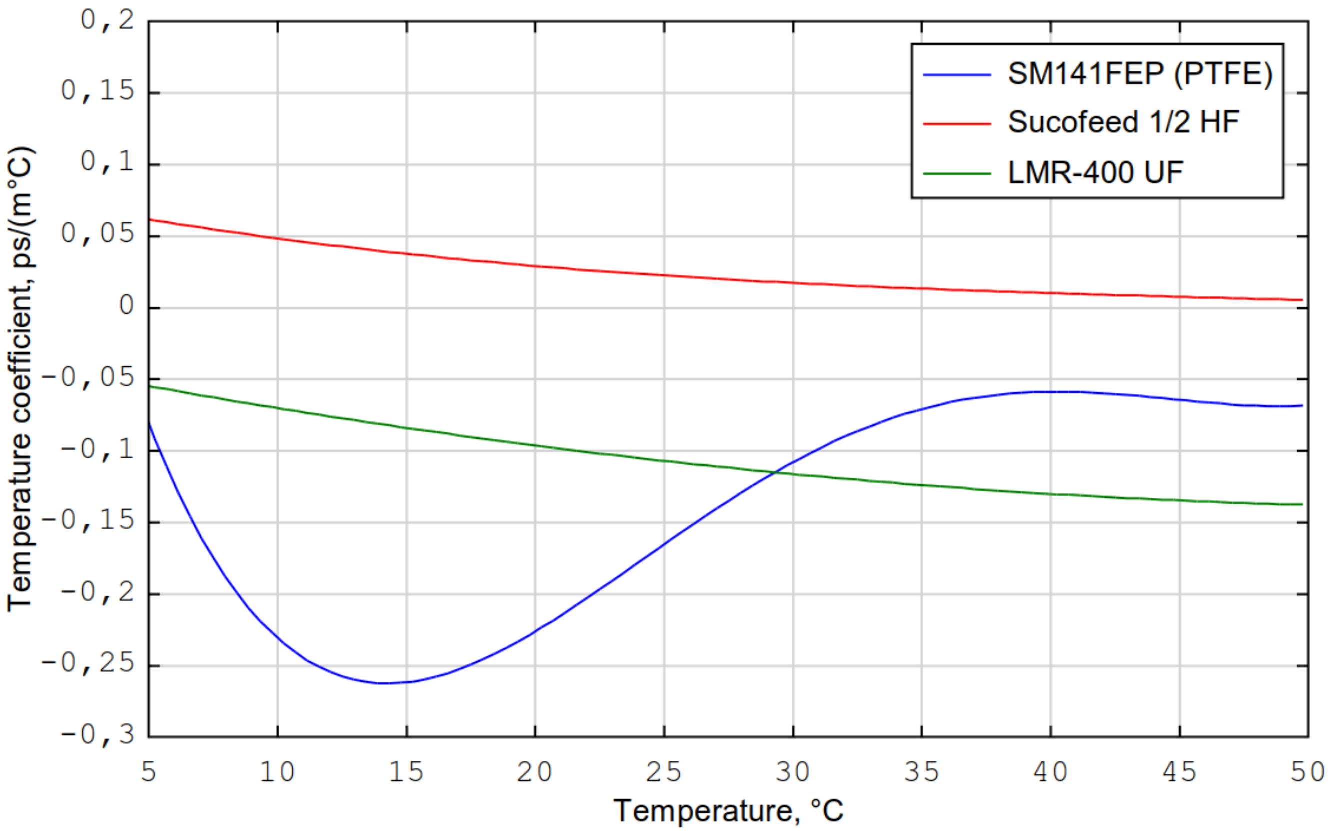
Group delay: tens to hundreds of ps

No data about TC, but probably it **<< 1 ps/K**

In total, $TC_{FrontEnd} \ll 1ps/K$

Measurements of BRAS frontend show TC in range of 0.1-0.2 ps/K depending on frequency.

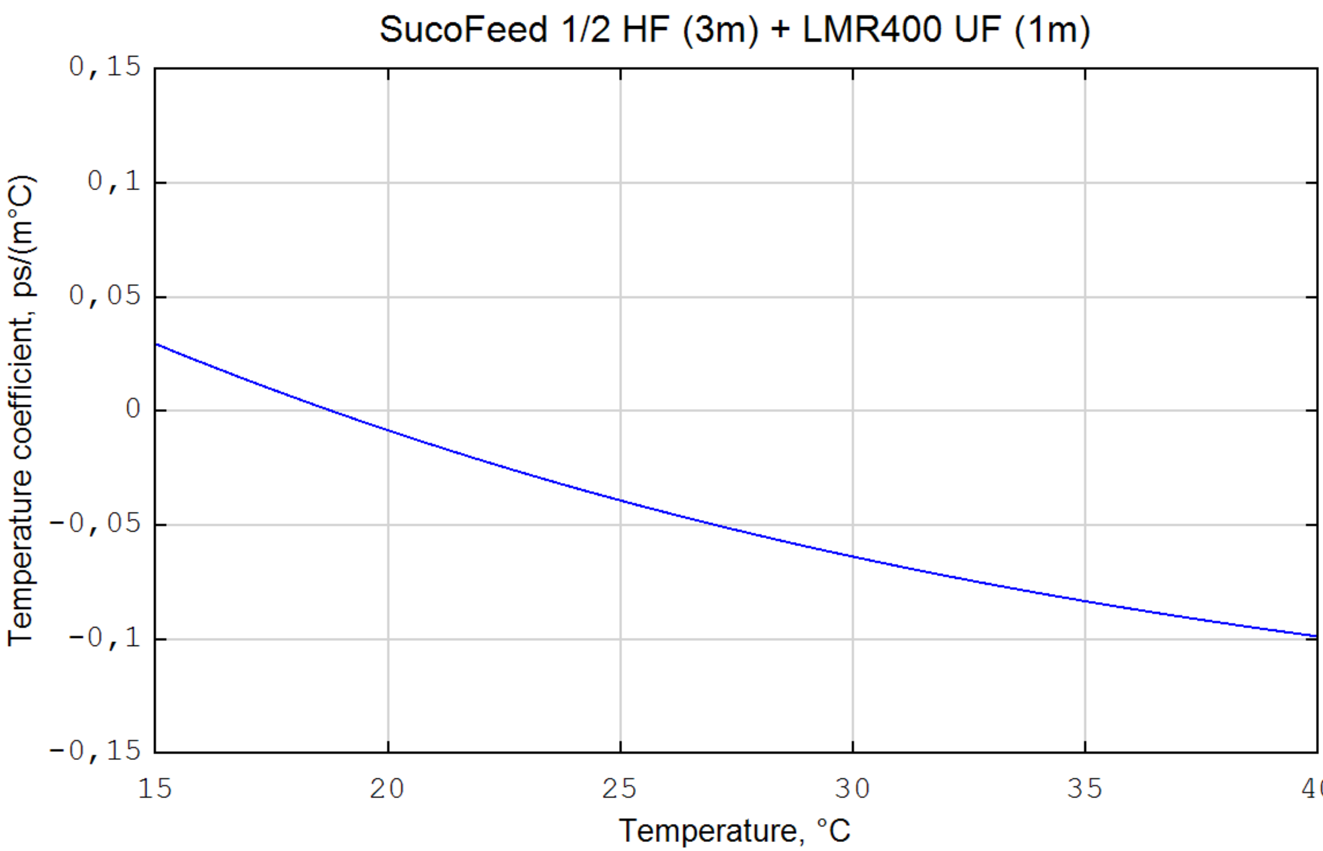
Temperature coefficient of delay in coaxial cables



Measured by D. Marshalov and A. Berdnikov in IAA RAS

15 cm of SM141FEP at room temperature (22 °C) has TC = 30 fs/K

Temperature coefficient of delay in IF cables to MDBE (RT13)



The cable from receiver to MDBE in RT-13 (Svetloe) consists of 2 pieces:

- 3 meters of SucoFeed ½ HF (mounted in cable tray)
- 1 meter of LMR400 UF (removable)

The total TC of the assembly is less than 0.1 ps/K

Temperature coefficient of delay in PCB traces

Propagation delay in stripline: $Tpd \approx \frac{\sqrt{\varepsilon_r}}{c} \quad {}^{s}/_{m}$

Length of PCB traces from reference clock input to ADC clock input in MDBE is about 40 cm

FR4

$\varepsilon_r \approx 4.5$

$TC_{\varepsilon_r} \approx 400\ ppm/K$ (*John Coonrod*. "Understanding When To Use FR-4 Or High Frequency Laminates". Onboard Technology, Sept. 2011)

$TC_{PCB} \approx 0.6\ ps/K$

Rogers RO4350B (used in MDBE for clock and high-speed lines)

$\varepsilon_r \approx 3.66$

$TC_{\varepsilon_r} \approx 50\ ppm/K$ (RO4350B datasheet)

$TC_{PCB} \approx 0.06\ ps/K$

Temperature coefficient of delay in clock distributors

In DBE with a few ADCs we need to distribute sampling clock signal to each of them. With more than 2 ADCs – specialized clock fanout IC is the choice.

Examples of clock distributors:

Part number	$\mathbf{TC_{dist}, fs/K}$
AD9508	2800
ADCLK854	2000
MAX9312	500
LTC6953	350
SY89112U	150
SY58034U	65
ADCLK954	50
NB7L1008M	35

TC of clock distributors depends on the rise time of input signal!

100 MHz sine wave (+10 dBm) on the input of ADCLK954 gives TC around 0.6 ps/K

Temperature coefficient of delay in clock synthesizers

TC of PLL-based clock synthesizers depends on:

1. Reference clock rise time
2. Particular PLL IC and settings

It's hard to predict TC during design.

Synthesizers usually have TC in the range of **a few ps/K**.

ADC clock synthesizer of BRAS has $TC_{Synt} \approx 1.2\ ps/K$ – not bad, but could be better

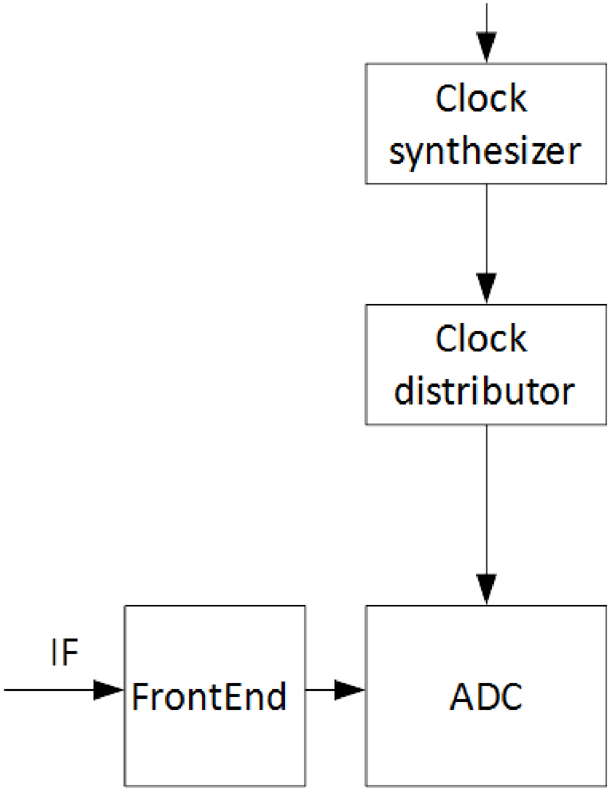
First version of clock synthesizer for MDBE will be measured in May 2019.

Temperature coefficient of delay in ADC

Ooops, no data at the moment

The measurements are scheduled for the end of 2019

Temperature coefficient of some abstract DBE



TC_{synt} $1.2\ ps/K$

TC_{dist} $2\ ps/K$

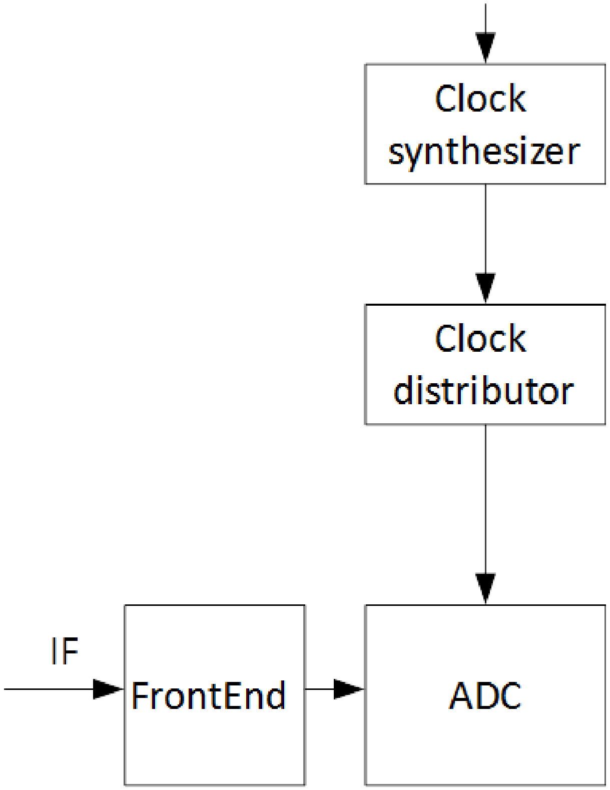
TC_{PCB} $0.6\ ps/K$

TC_{ADC} $???\ ps/K$

TC_{DBE} $3.8 + ???\ ps/K$ $TC_{BRAS} \approx 4.5\ ps/K$

To keep delay variations in BRAS less than 1 ps
temperature variations should be less than ± 0.1℃ !

Prediction of MDBE temperature coefficient



TC_{synt} $???\ ps/K$

TC_{dist} $0.05\ ps/K$

TC_{PCB} $0.06\ ps/K$

TC_{ADC} $???\ ps/K$

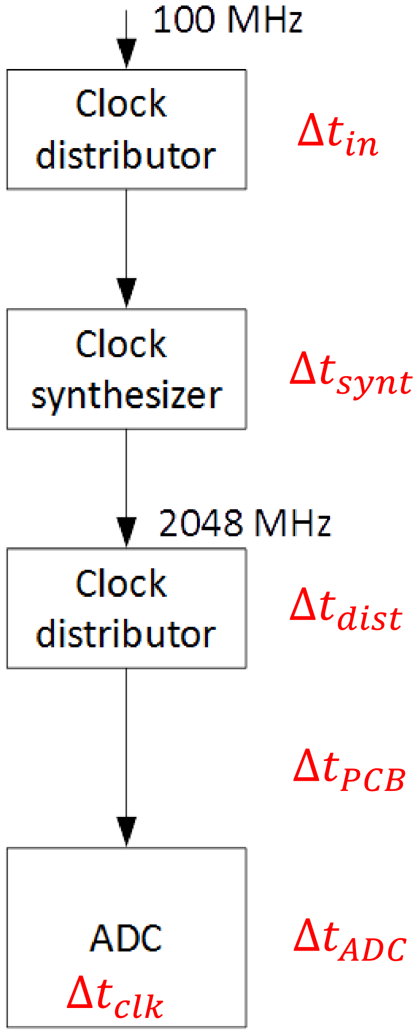
TC_{MDBE} $0.11 + ???\ ps/K$

Too many unknowns!

The developer can decrease TC by careful design but he can not predict the resulting total TC until we measure it in a real device.

How do we measure it?

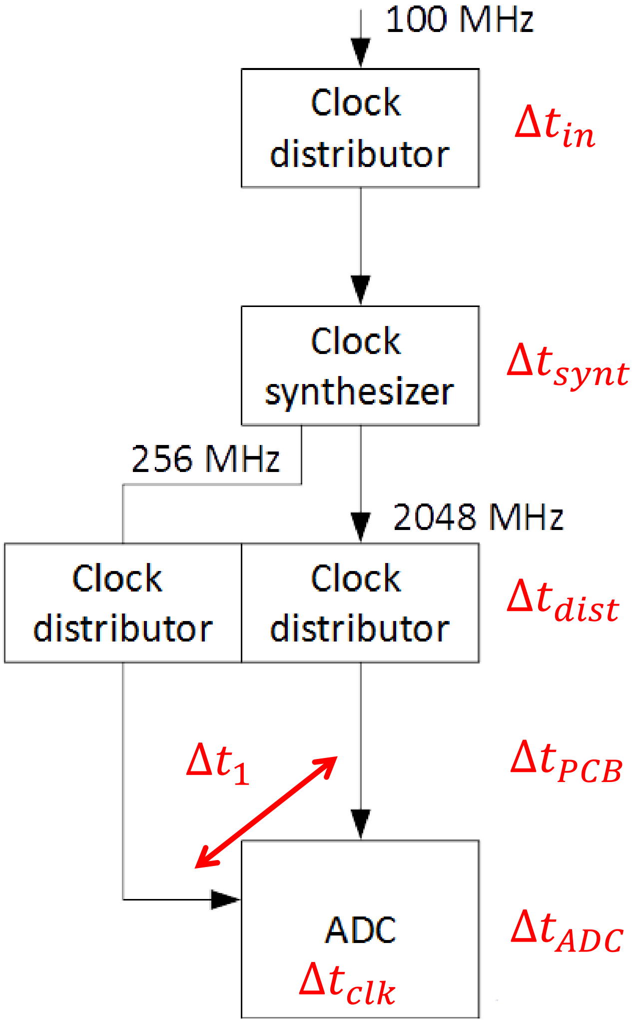
Embedded delay measurement circuits in MDBE



Variations of ADC (formatter) clock in MDBE consist of:

$$\Delta t_{clk} = \Delta t_{in} + \Delta t_{synt} + \Delta t_{dist} + \Delta t_{PCB} + \Delta t_{ADC}$$

Embedded delay measurement circuits in MDBE



ADC requires calibration signal to tune gain, offset and phase of the cores.

Calibration signal is measured by PCAL extractor unit in FPGA.

Measured variations of calibration signal include:

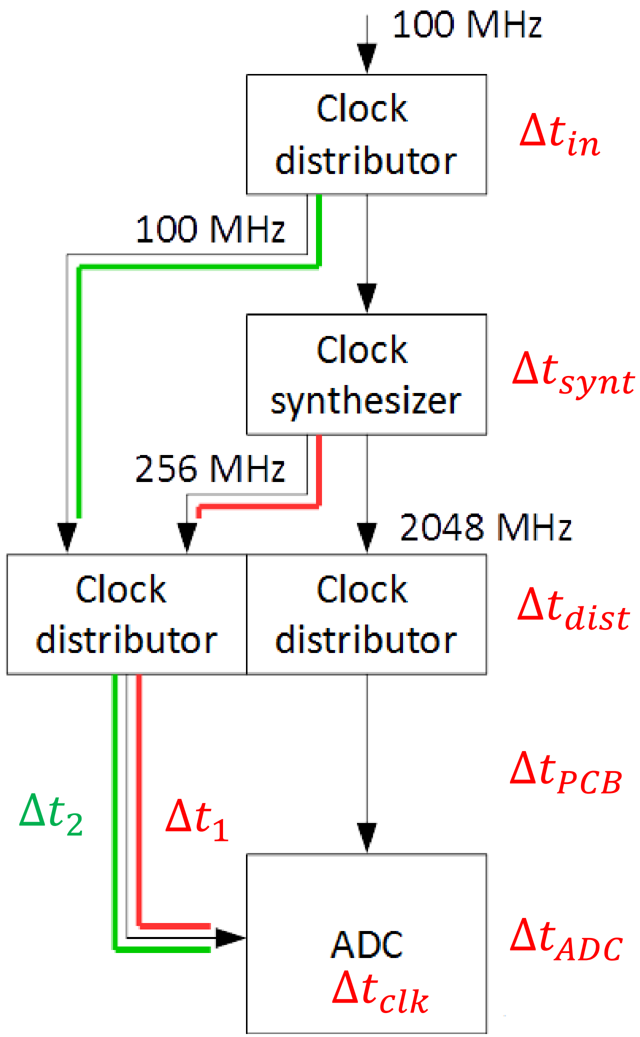
$$\Delta t_1 = \Delta t_{in} + \Delta t_{synt} + \Delta t_{dist} + \Delta t_{PCB} - \Delta t_{clk}$$

where variations of ADC clock:

$$\Delta t_{clk} = \Delta t_{in} + \Delta t_{synt} + \Delta t_{dist} + \Delta t_{PCB} + \Delta t_{ADC}$$

$$\Delta t_1 = -\Delta t_{ADC}$$

Embedded delay measurement circuits in MDBE



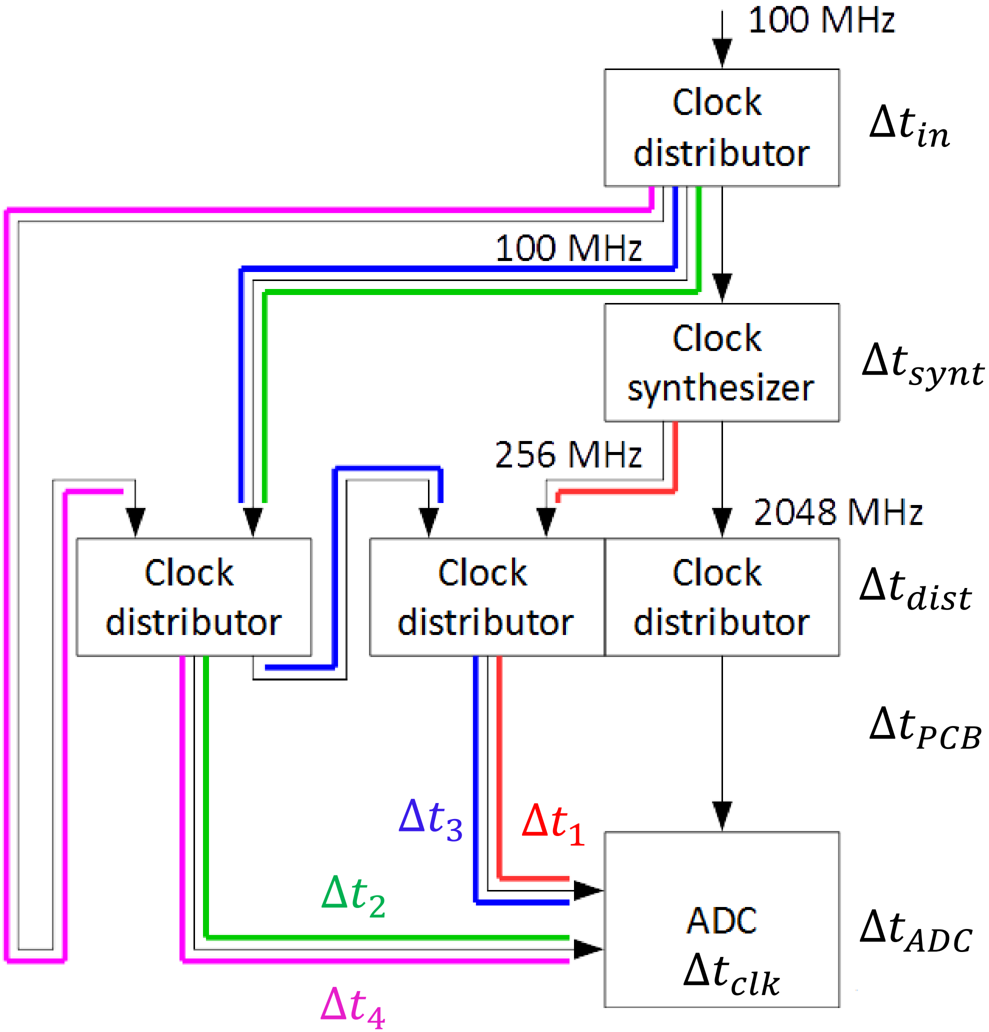
$$\Delta t_2 = \Delta t_{in} + \Delta t_{dist} + \Delta t_{PCB} - \Delta t_{clk}$$

$$\Delta t_2 = -\Delta t_{synt} - \Delta t_{ADC}$$

$$\Delta t_1 = -\Delta t_{ADC}$$

$$\Delta t_{synt} = \Delta t_1 - \Delta t_2$$

Embedded delay measurement circuits in MDBE



$$\Delta t_1 = -\Delta t_{ADC}$$

$$\Delta t_2 = -\Delta t_{synt} - \Delta t_{ADC}$$

$$\Delta t_3 = \Delta t_{in} + 2\Delta t_{dist} + \Delta t_{PCB} - \Delta t_{clk}$$

$$\Delta t_3 = -\Delta t_{synt} + \Delta t_{dist} - \Delta t_{ADC}$$

$$\Delta t_4 = \Delta t_{in} + \Delta t_{dist} + 2\Delta t_{PCB} - \Delta t_{clk}$$

$$\Delta t_4 = -\Delta t_{synt} + \Delta t_{PCB} - \Delta t_{ADC}$$

$$\Delta t_{ADC} = -\Delta t_1$$

$$\Delta t_{synt} = \Delta t_1 - \Delta t_2$$

$$\Delta t_{dist} = \Delta t_3 - \Delta t_2$$

$$\Delta t_{PCB} = \Delta t_4 - \Delta t_2$$

Summary

- VLBI digital backends in general can have temperature coefficient of delay in the range of a few ps/K – noticeably for VGOS applications.

- Temperature coefficient of a digital backend has to be measured and specified in datasheet

- Special care should be taken during backend design to keep its temperature coefficient low. But even though, you never know it in advance unless you had prototyped all parts in advance.

- To simplify the measurements of internal delays variations, MDBE has specialized circuits. In case of success, it will allow to control the delay stability in the sensitive parts of MDBE. It, in turn, makes possible to use MDBE as self-calibrated multichannel instrument for measuring stability of other devices.

Thank you!

Questions?