Connecting iBOBs to the eMerlin Correlator

 8^{th} International eVLBI Workshop, Madrid, 22^{nd} – 26 June 2009

J Hargreaves Jodrell Bank Observatory/JIVE

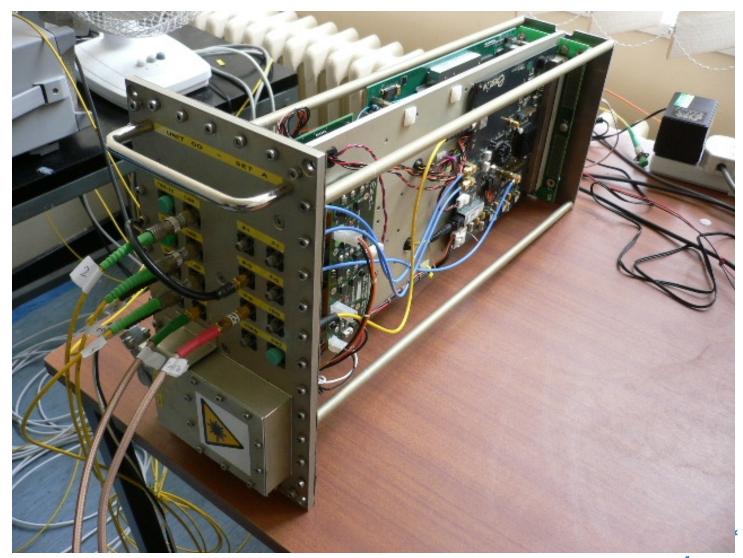


Introduction

- eMerlin correlator hardware & iBOB connection
- Station Board configuration
- eMerlin import from Onsala
- Data flow control

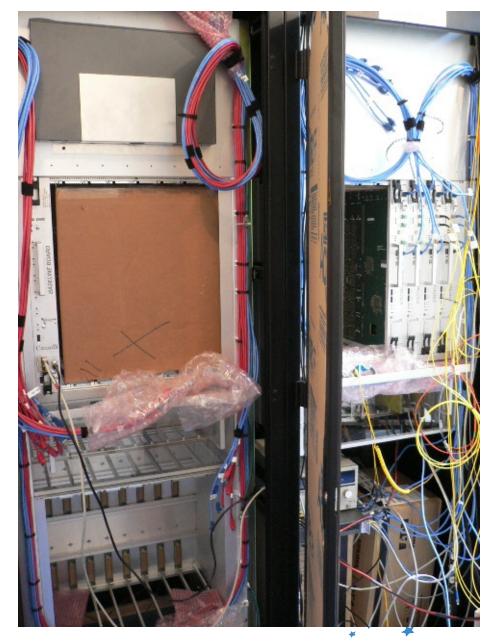


DINT – <u>D</u>igitizer <u>In</u> <u>T</u>elescope



Racks

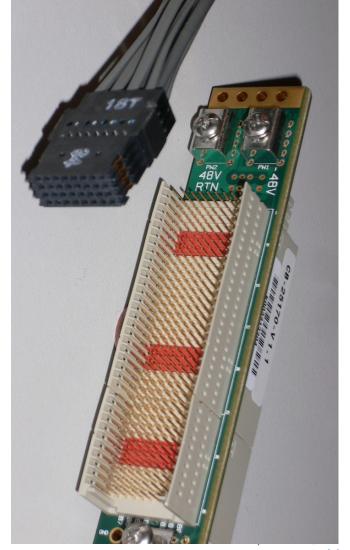
- •At left baseline rack with one board
- •There is space for 16
- At right station rack with 4 Station Boards out of 8 populated
- Under this a 6U rack for crossbar boards and iBOBs





Station Board Backplane





iBOB with Adaptor cards

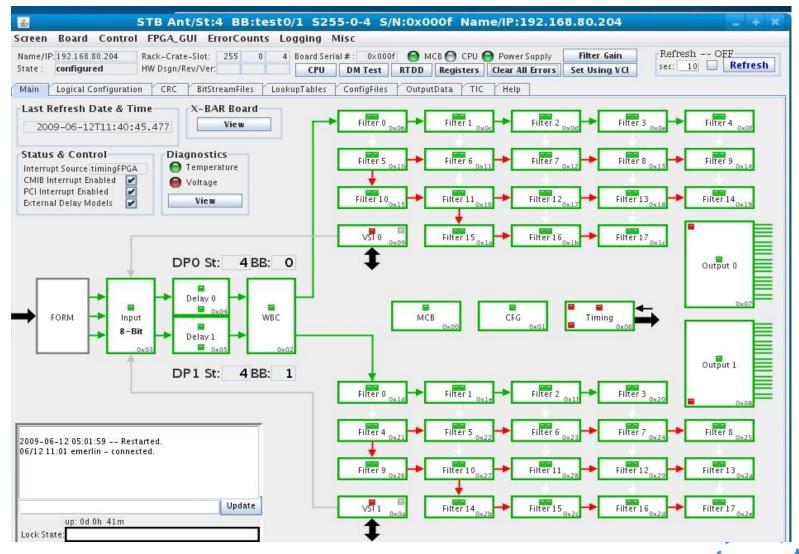


iBOB Backplane Connector

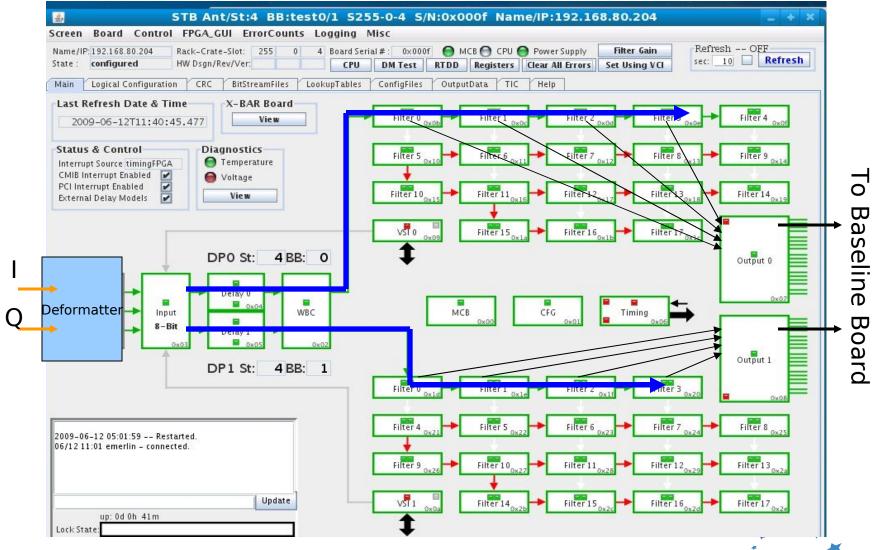




Station Board Signal Flow



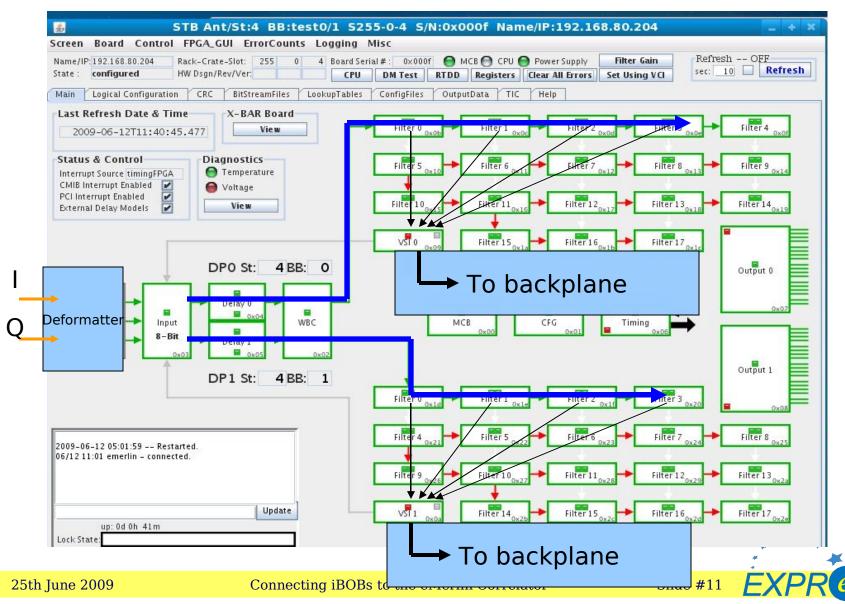
SB Signal Flow – Local Data



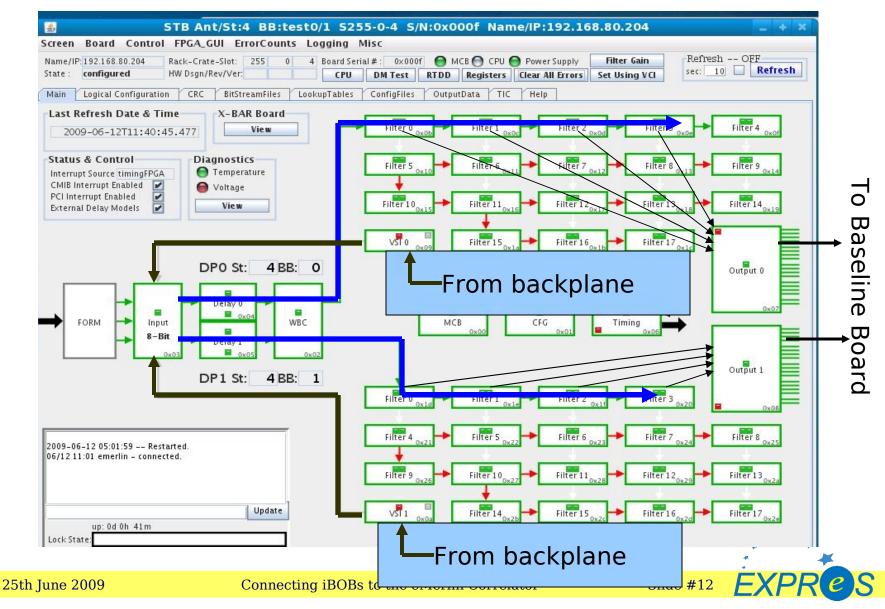
SB Signal Flow – 8 bit data

organisation 63 b7 STB Ant/St:4 BB:test0/1 S255-0-4 Screen Board Control FPGA_GUI ErrorCounts Logging Misc Earliest I sample Name/IP: 192.168.80.204 Rack-Crate-Slot: 4 Board Serial # : b0 efresh configured HW Dsgn/Rev/Ver: CPU DM Test h7 Logical Configuration CRC BitStreamFiles LookupTables Configliles Earliest Q sample Last Refresh Date & Time X-BAR Board b0 View 2009-06-12T11:40:45.477 h7 Status & Control Diagnostics Filter 5 Temperature Interrupt Source timingFPGA b0 CMIB Interrupt Enabled Voltage PCI Interrupt Enabled h7 Filter 10 Vie w External Delay Models Baseline b0 VST 0 h7 DP0 St: 4 BB: 0 b0 h7 Deformatter WBC Input Board 8-Bit b0 h7 4 BB: 1 Latest I sample DP1 St: Filter v b0 b7 Latest Q sample Filter 4 2009-06-12 05:01:59 -- Restarted. 06/12 11:01 emerlin - connected. b0 Filter 9 Both 64 bit data VSI 1 Update up: 0d 0h 41m paths are identical Lock State:

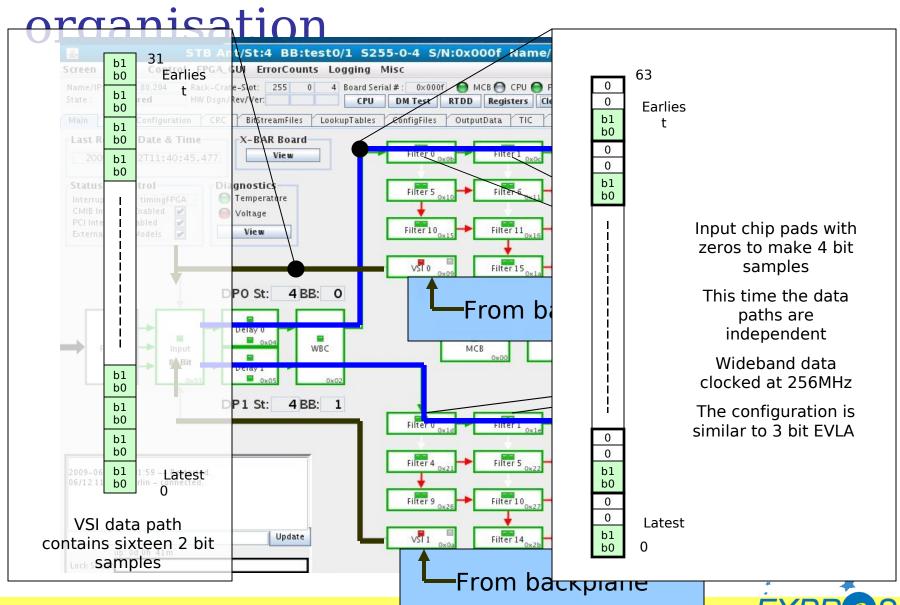
SB Signal Flow – eMerlin Export



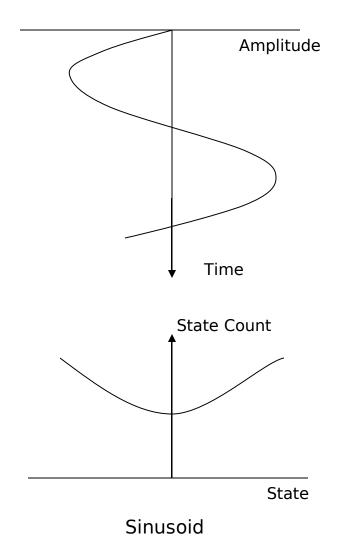
SB Signal Flow – eMerlin Import

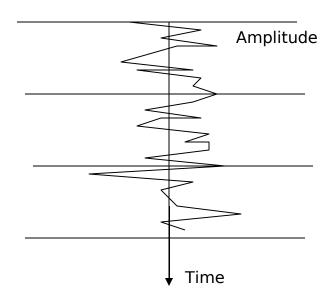


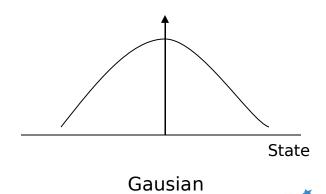
SB Signal Flow – VSI data



State Count Histograms

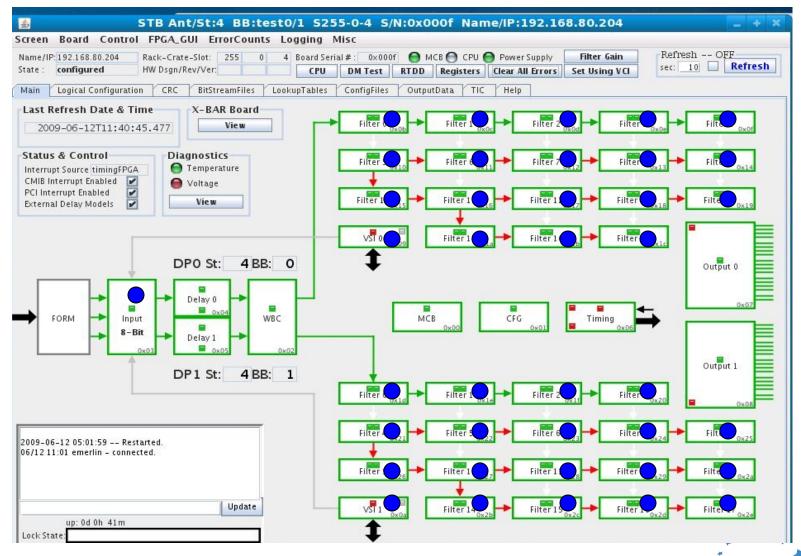




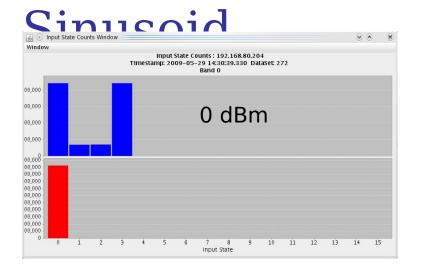


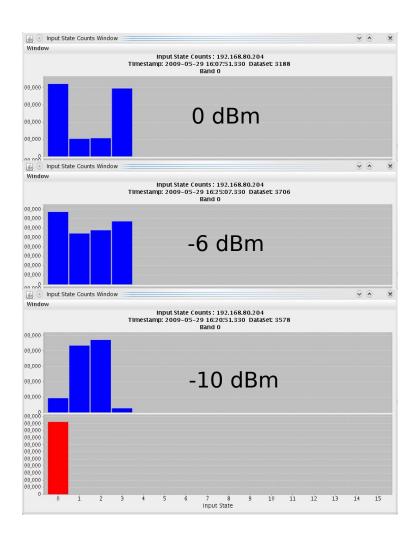


Station Board State Counts



Input Chip State Counts 88MHz

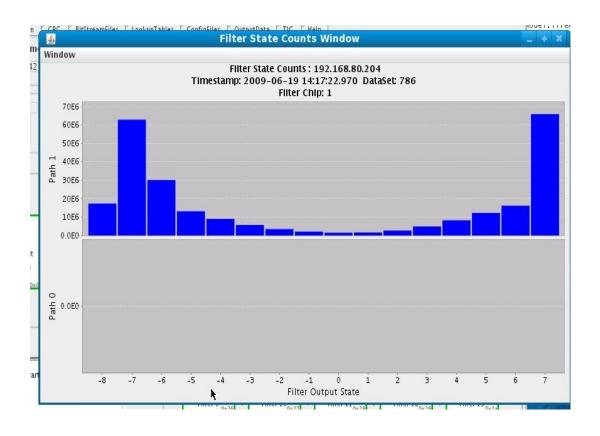




Data from Onsala via Network

#16 EXPRES

Filter Chip State Counts



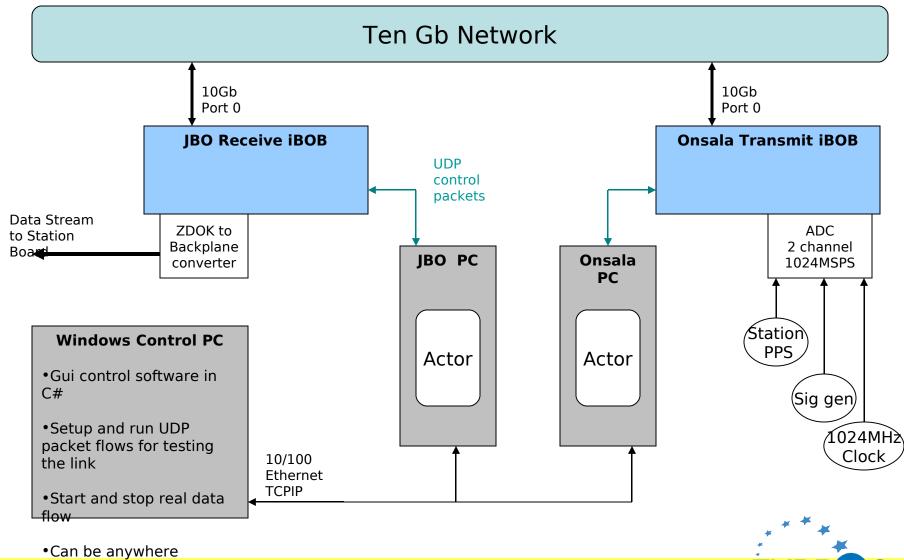
Filter chip output

Data source is 88MHz, -6dBm sinusoid at Onsala

SB configured as for 3 bit EVLA



iBOB Control (RHJ)



iBOB Control Register

- 32 bit register allows software control over FPGA fabric
- Interface is common to iNetTest and data flow

iBOB Control Register

Bit	Use
0 1 2 3 4 5 6 7 8 9 10- 31	Arm – start test flow on next PPS Not used One shot – start test flow immediately Cancel burst – return transmitter to idle state Reset Counters – reset statistics counters Histogram enable – Event enable Send data Set realtime Latch Time Not used

iBOB Status Register

Bit	Use
0-15 16- 23 24- 28 29 30 31	Packet size from MAC Receiver state Not used Real time done – 1 when time has been set Sending – 1 when transmitting packets Control pkt – 0 = data, 1 = control packet

Questions/Answers

- Contact information
 Dr Jonathan Hargreaves
 Electronic Engineer
 Jodrell Bank Observatory
 jh@jb.man.ac.uk
- Additional Information
 http://expres-eu.org/ [note: only one "s"]
 http://www.jive.nl/
- EXPReS is made possible through the support of the European Commission (DG-INFSO), Sixth Framework Programme, Contract #026642