Design and fabrication of a fast, multi-bits analog-to-digital converter for astrophysics and cosmology applications

Diego Rossoni Mattos
Prof. Alain Baudry
Prof. Jean-Batiste Bégueret

Outline

- Scientific Context
- Motivation
- Features
- Block-Diagram
  - Track-and-Hold (T&H)
  - Input Buffer
  - Comparators
  - DFFs
  - Encoder
  - 1:4 Demultiplexer
  - LVDS Buffers
- Conclusion

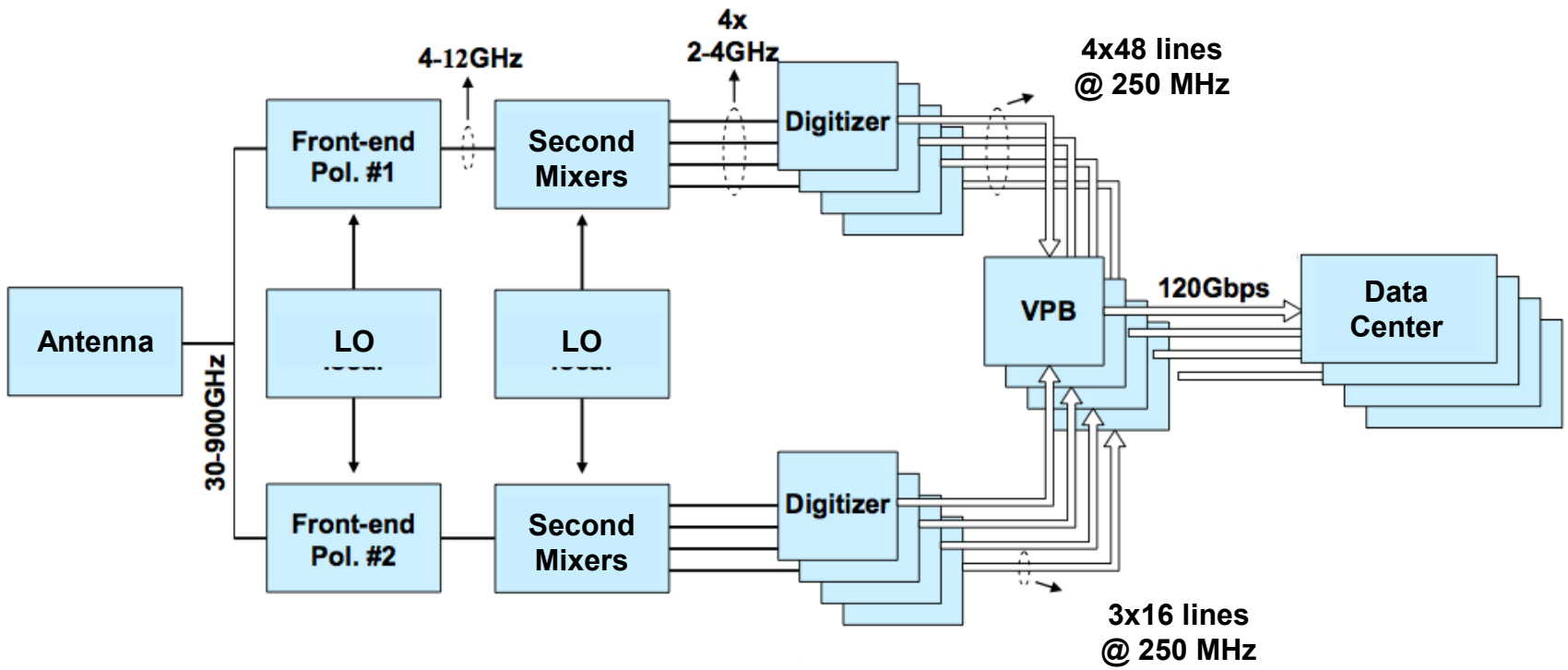
Scientific context

- Radio telescopes in millimeter and sub-millimeter wave domains
- Wide frequency bands to analyze
- Cosmology
  - Neutrino study
  - Gamma spectroscopy

Motivation

Device	Observation Band	Receiver Band	ADC Input Bandwidth	Sampling Frequency	Resolution
ALMA (Chile)	30-1000GHz	4-12 GHz (4 bands)	2-4 GHz	4 GHz	3 bits
EVLA (USA)	1-90 GHz	4-12 GHz (4 bands)		4 GHz	3 bits
IRAM (France)	80- 340 GHz	2-4 GHz	2-4 GHz		2 bits
ATCA (Australia)	1-105 GHz	4.5-11 GHz	1-2 GHz	2 interleaved 2 GHz	10 bits

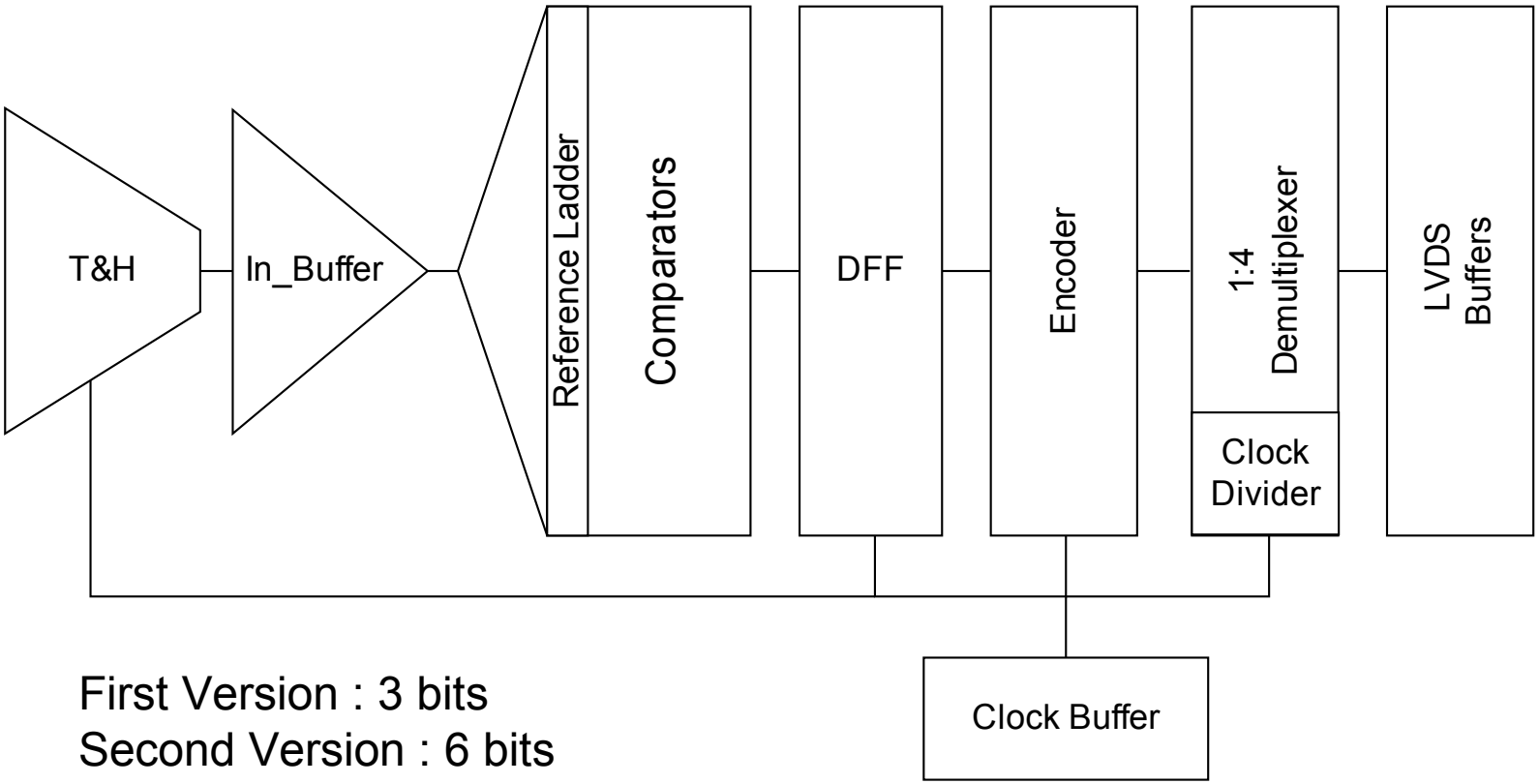
ALMA Architecture



Features

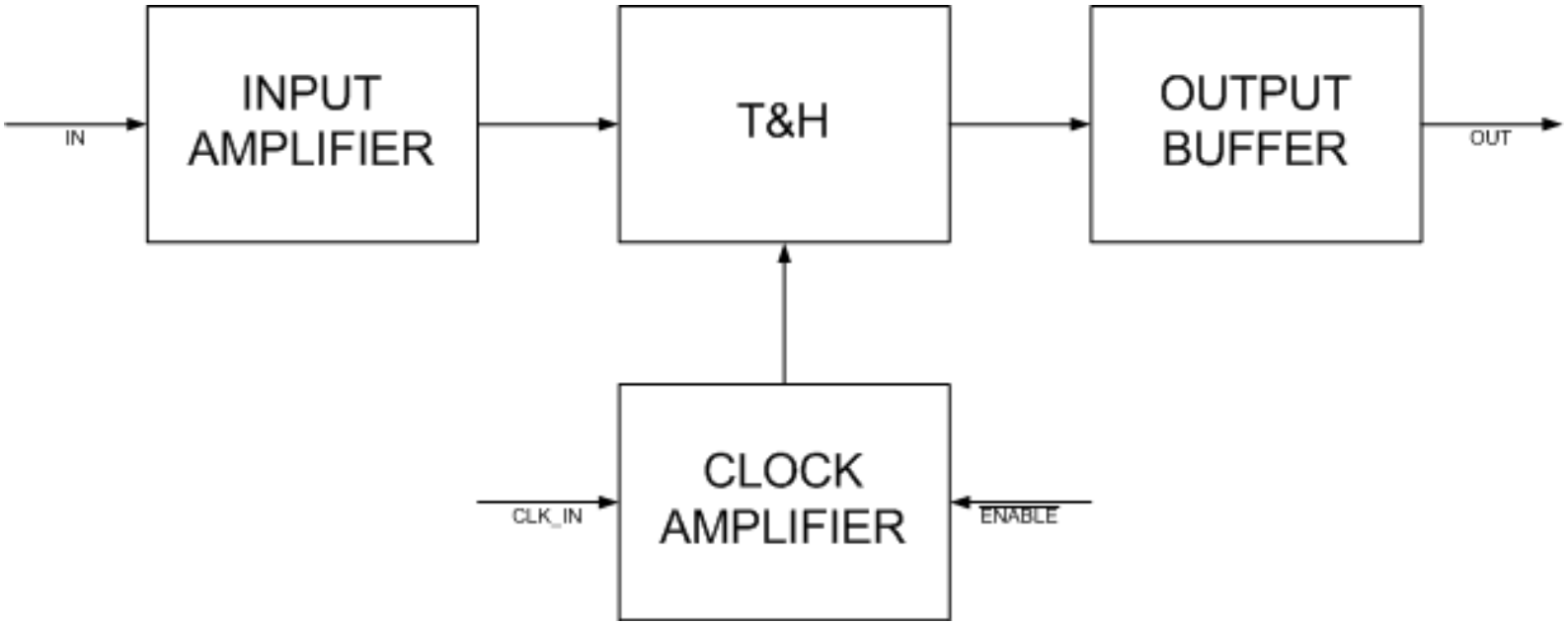
- Input Analog Bandwidth ➔ 8 GHz
- Sampling Frequency ➔ 8 GHz
- Resolution ➔ 6 bits
- Integrated Track-and-Hold
- 1:4 Integrated Demultiplexer
- LVDS Outputs
- CMOS 65 nm technology

Block Diagram

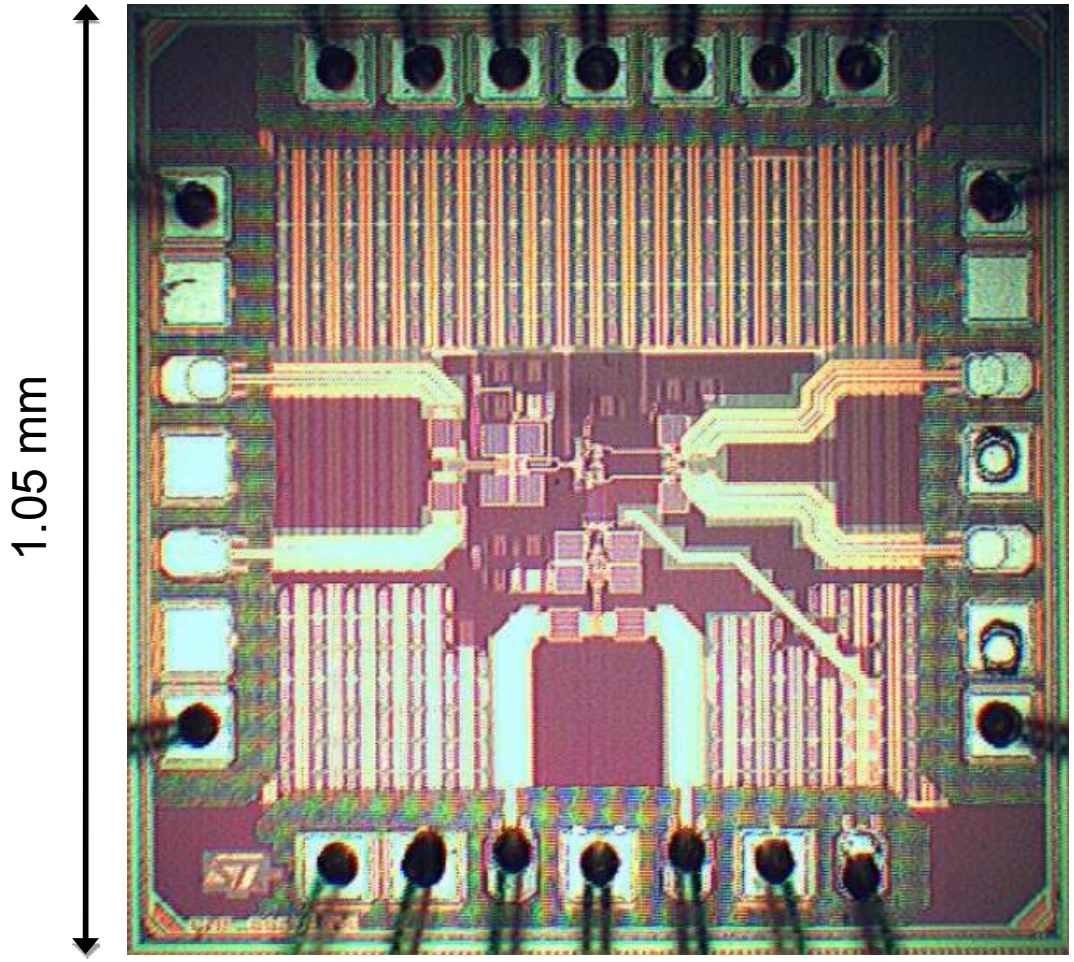


First Version : 3 bits
Second Version : 6 bits

T&H Block Diagram



T&H Layout



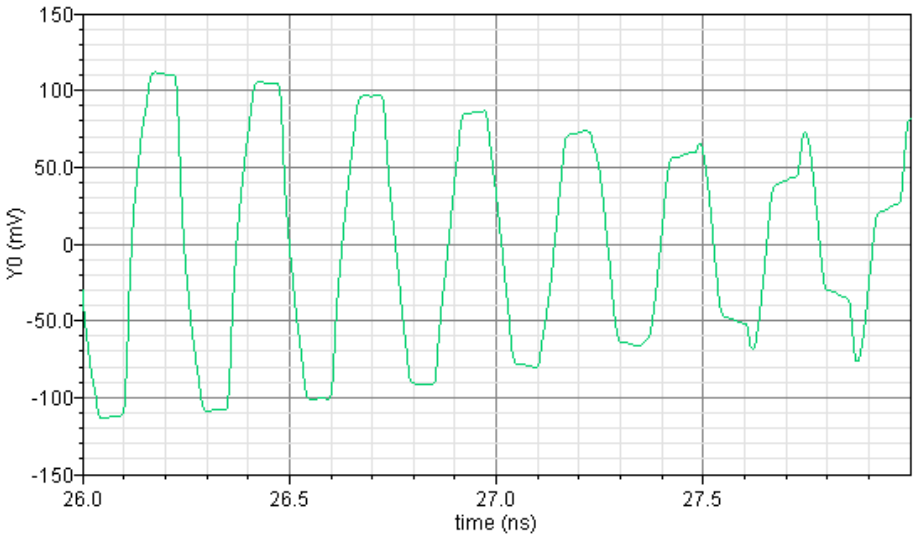
T&H Features

	Value	Unit
Sampling Frequency	8	GHz
Input Bandwidth	8	GHz
Power Consumption	160	mW
Gain	-2 to -4	dB
Input, Output and Clock Differential Impedance	100	Ω
Input, Output and Clock VSWR (at 8 GHz)	< 2	-
Hold-time	> 40	ps

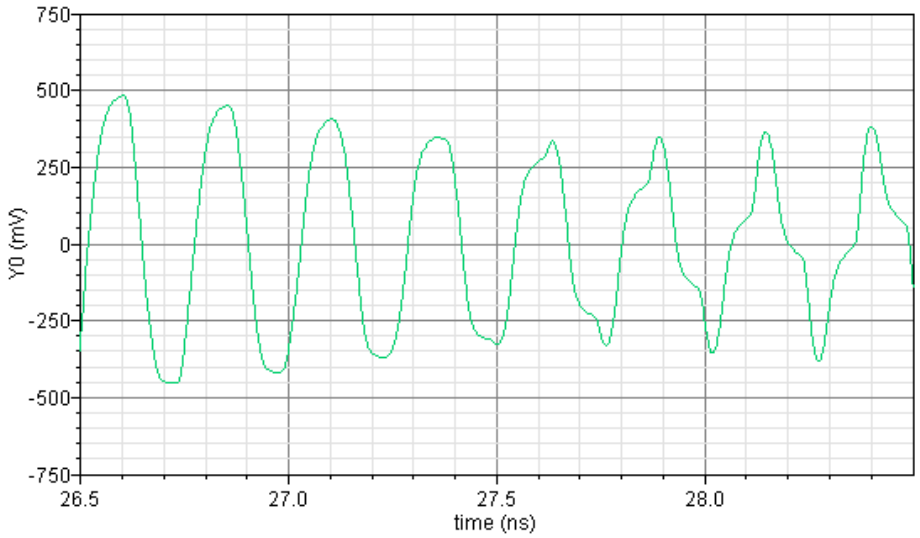
Input Buffer

- T&H output ➔ 100 mVpp
- ADC full scale ➔ 540 mVpp (~15 dB)

T&H Output

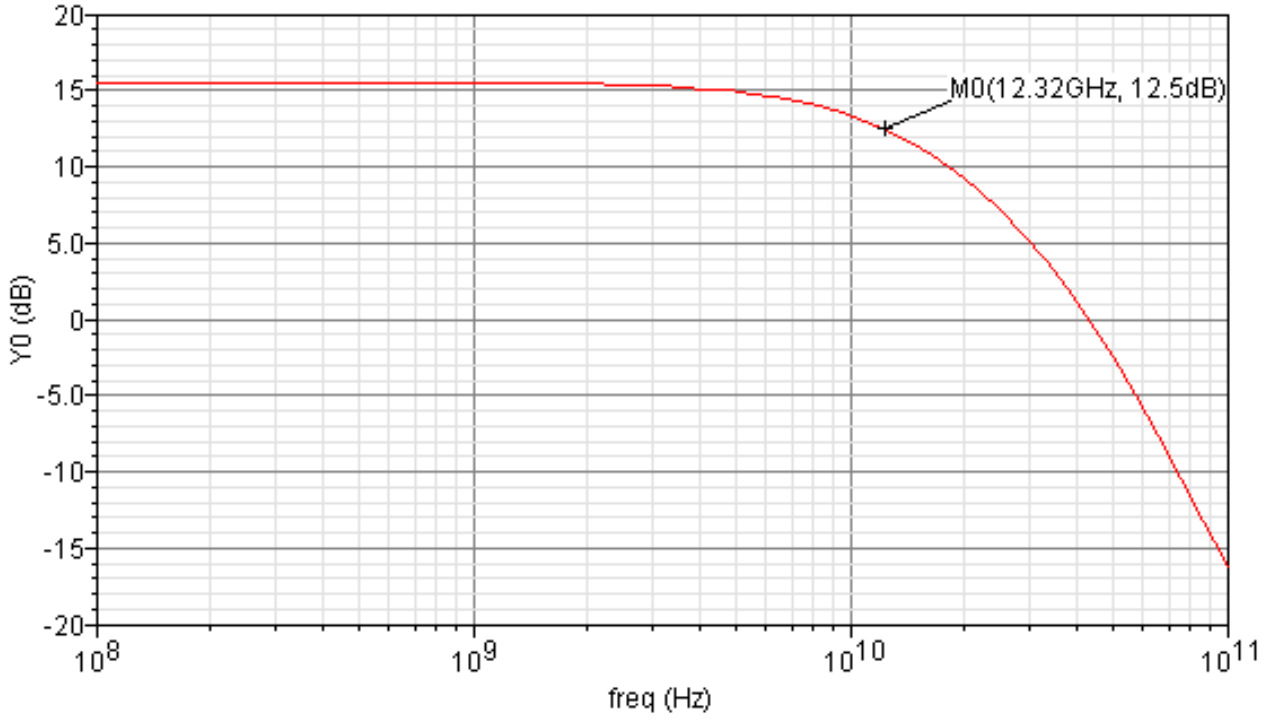


Input Buffer Output

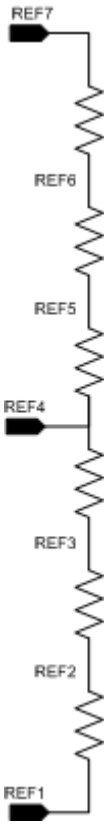


Input Buffer

Input Buffer Gain

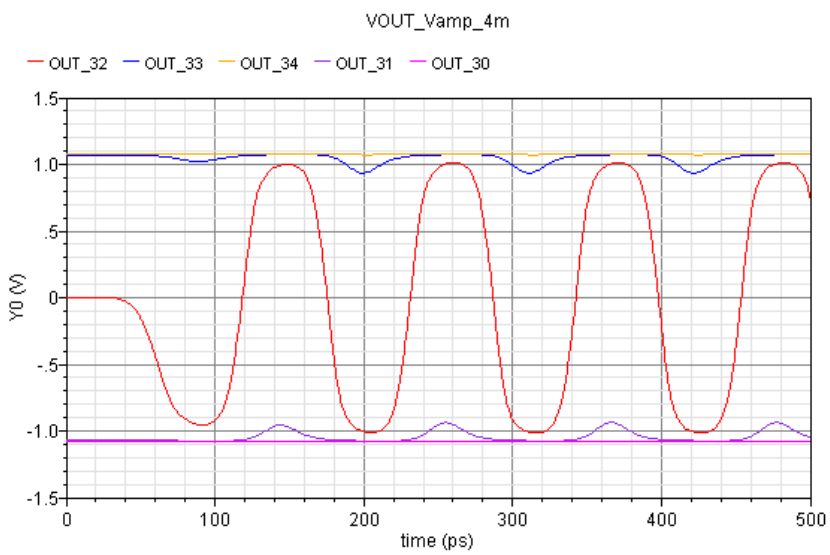


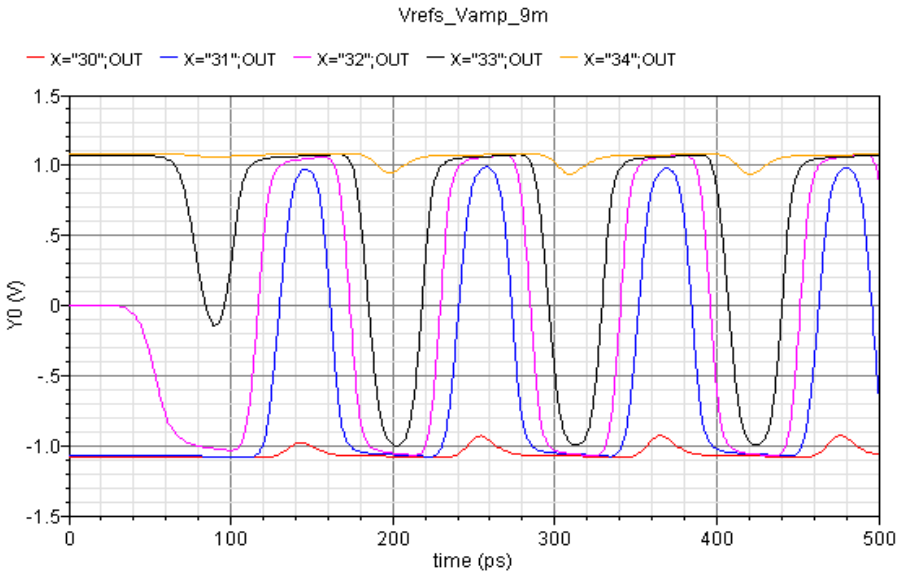
Comparator Reference Ladder

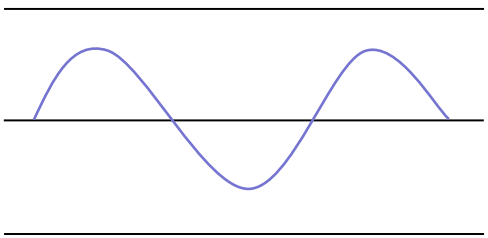


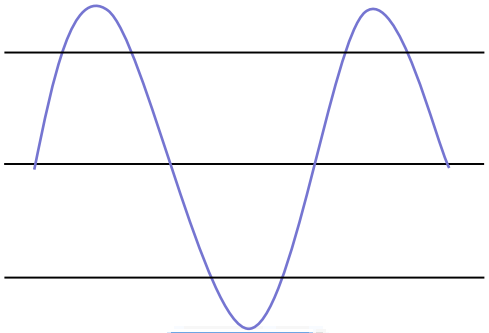
- 540 mV Full-scale
  - 77 mV between two references for 3 bits
  - 8,5 mV between two references for 6 bits
- Good layout to decrease mismatches

Comparator


VOUT_Vamp_4m
OUT_32
OUT_33
OUT_34
OUT_31
OUT_30
1.5
1.0
.5
0
-.5
-1.0
-1.5
Y0 (V)
0
100
200
300
400
500
time (ps)

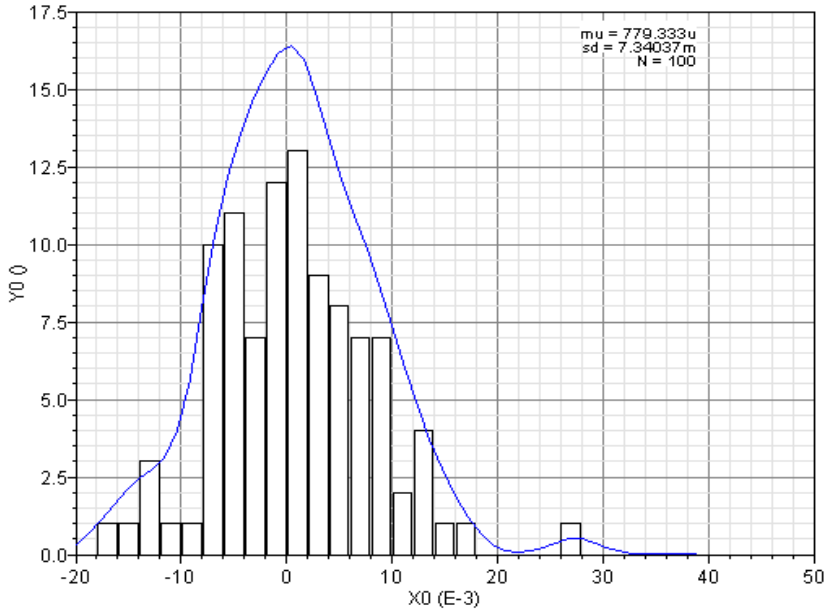

Vrefs_Vamp_9m
X="30";OUT
X="31";OUT
X="32";OUT
X="33";OUT
X="34";OUT
1.5
1.0
.5
0
-.5
-1.0
-1.5
Y0 (V)
0
100
200
300
400
500
time (ps)



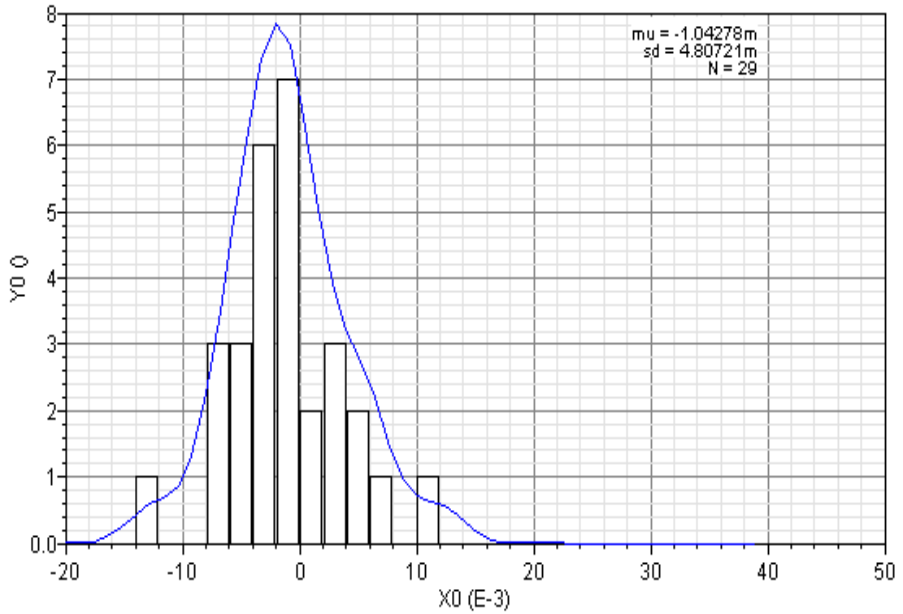


Comparators Offset

Offset variation

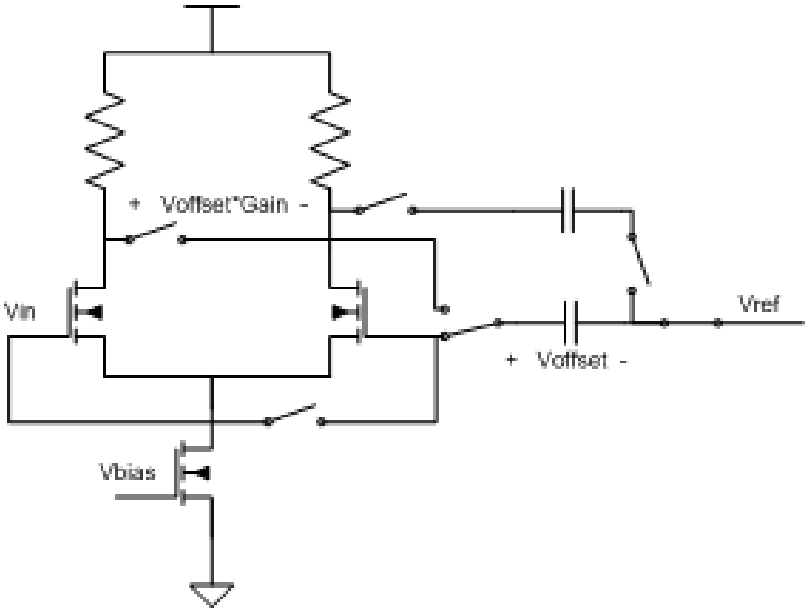


Offset variation

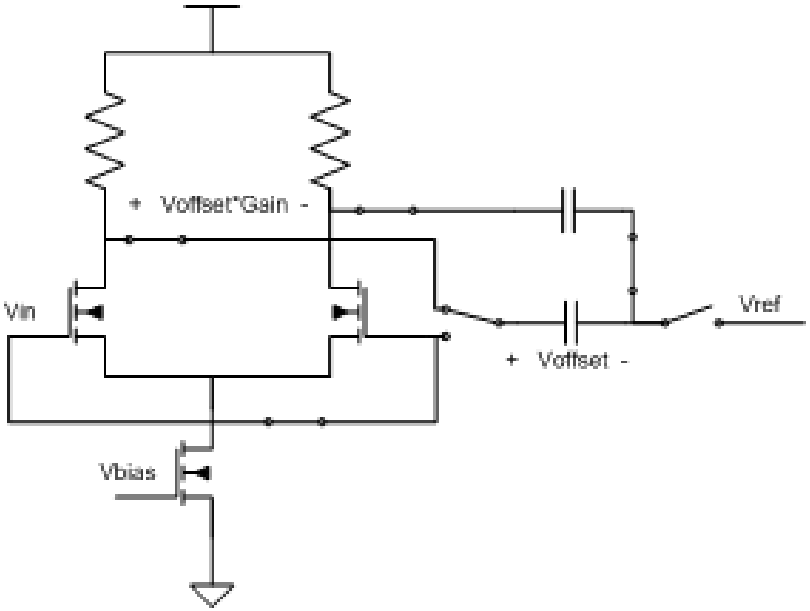


Offset Correction System

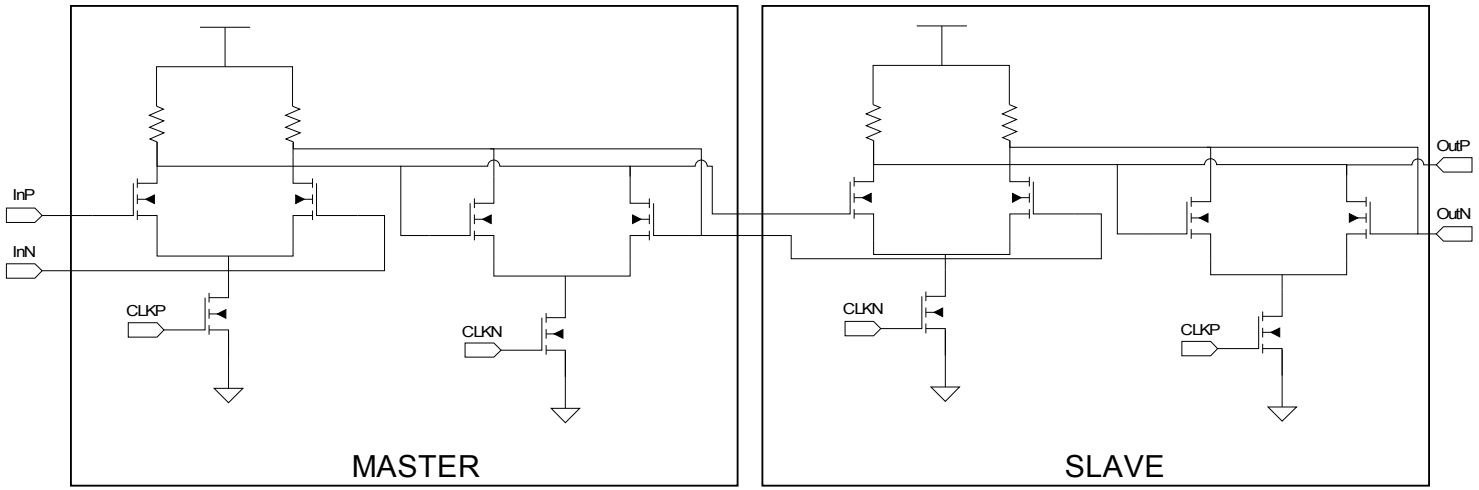
- Phase 1



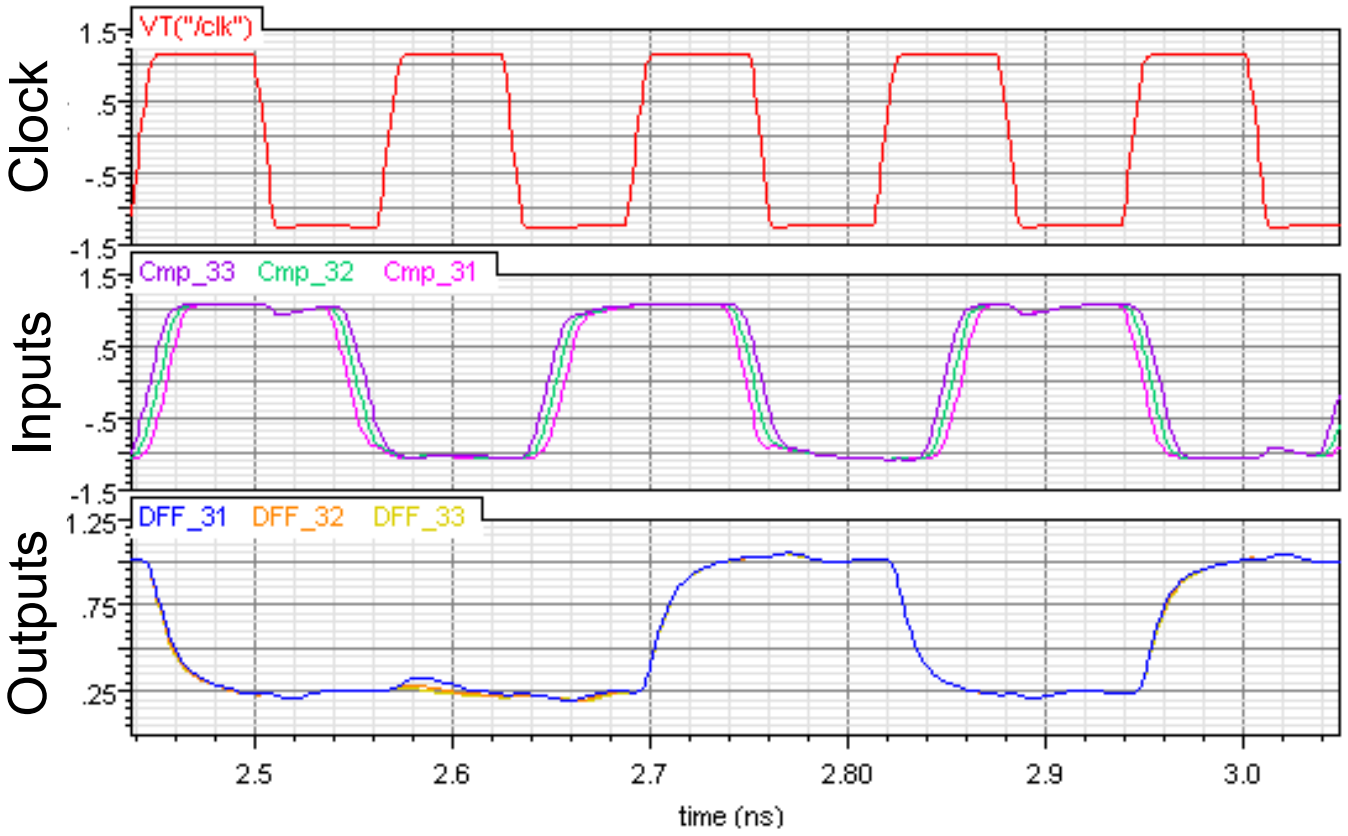
- Phase 2



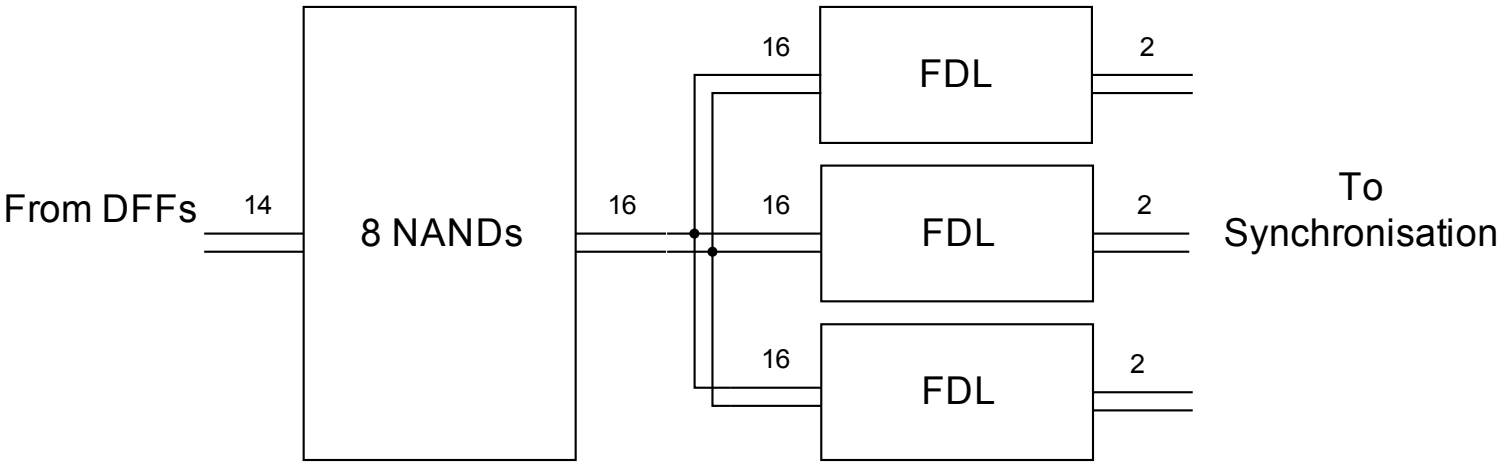
Differential Flip-Flop



Differential Flip-Flop

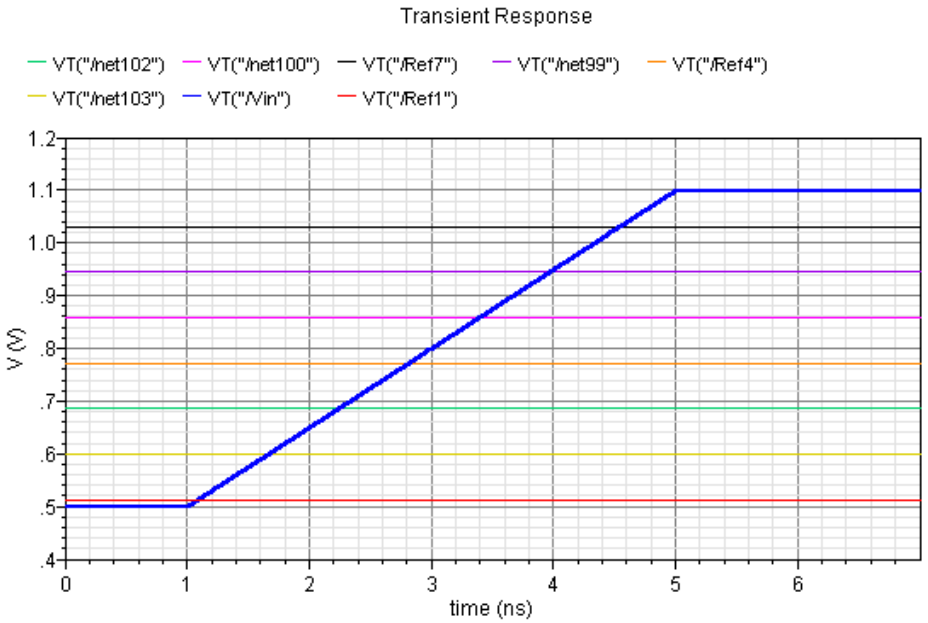


Encoder Architecture

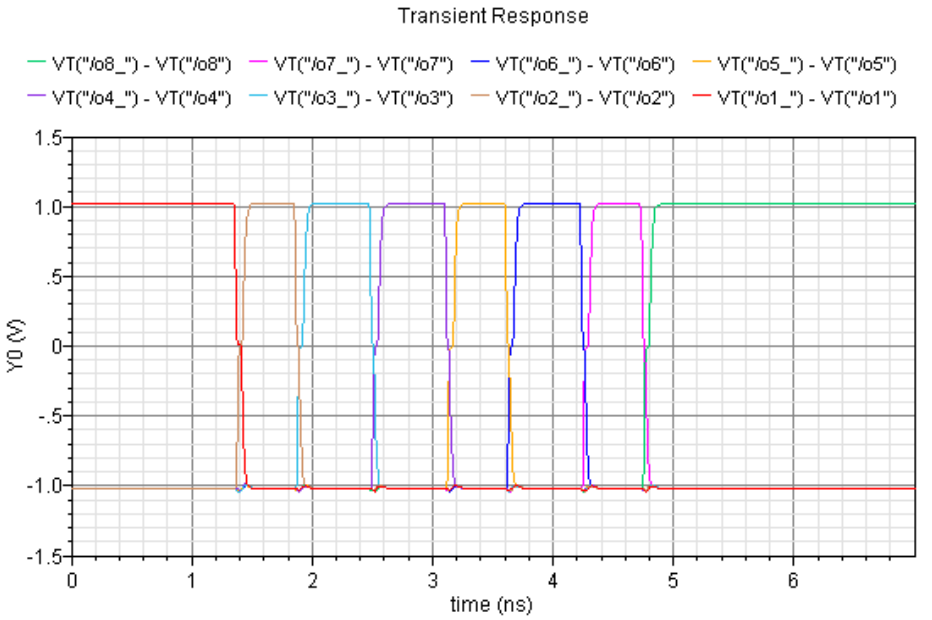


Encoder

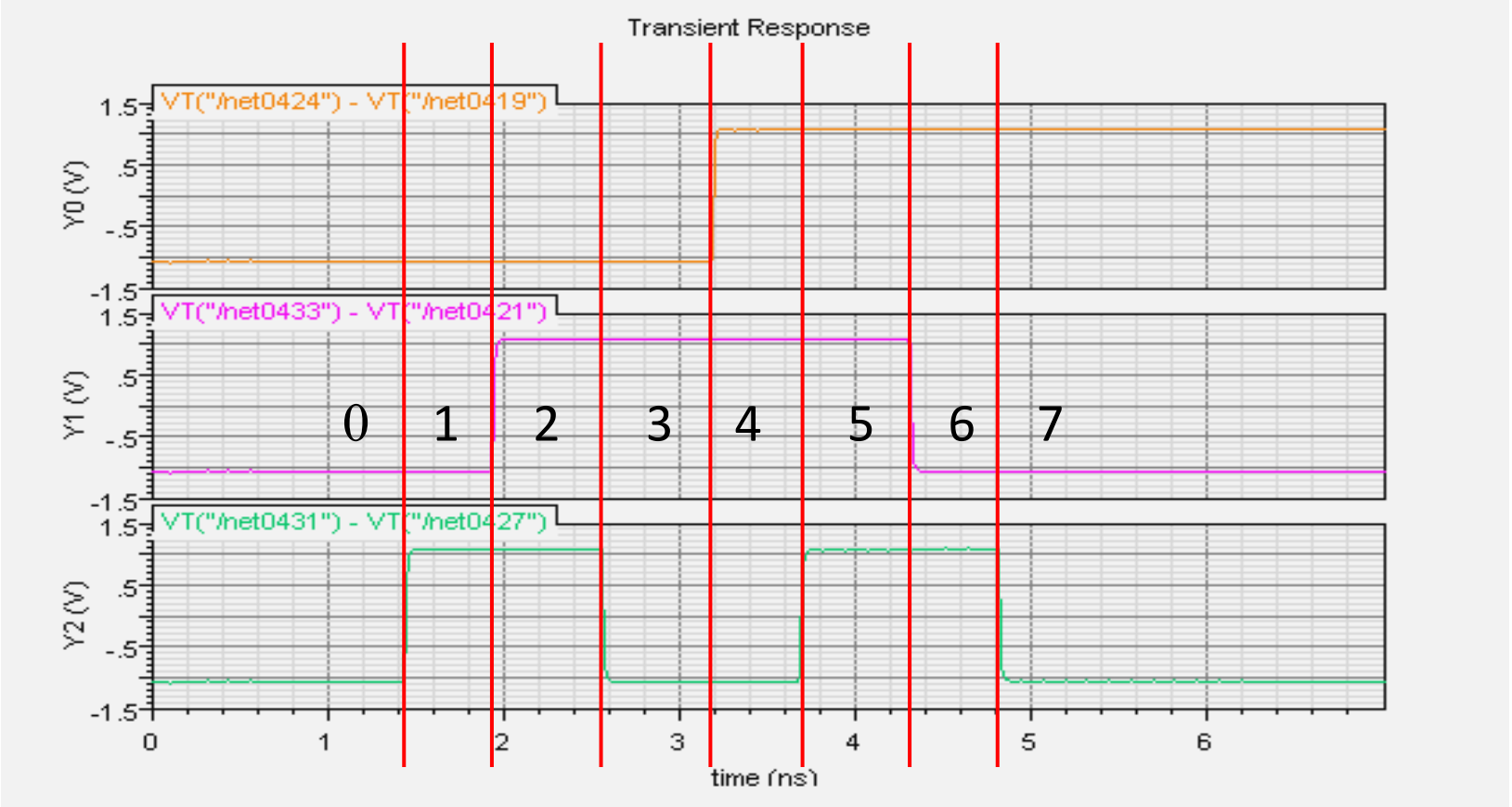
Circuit Inputs



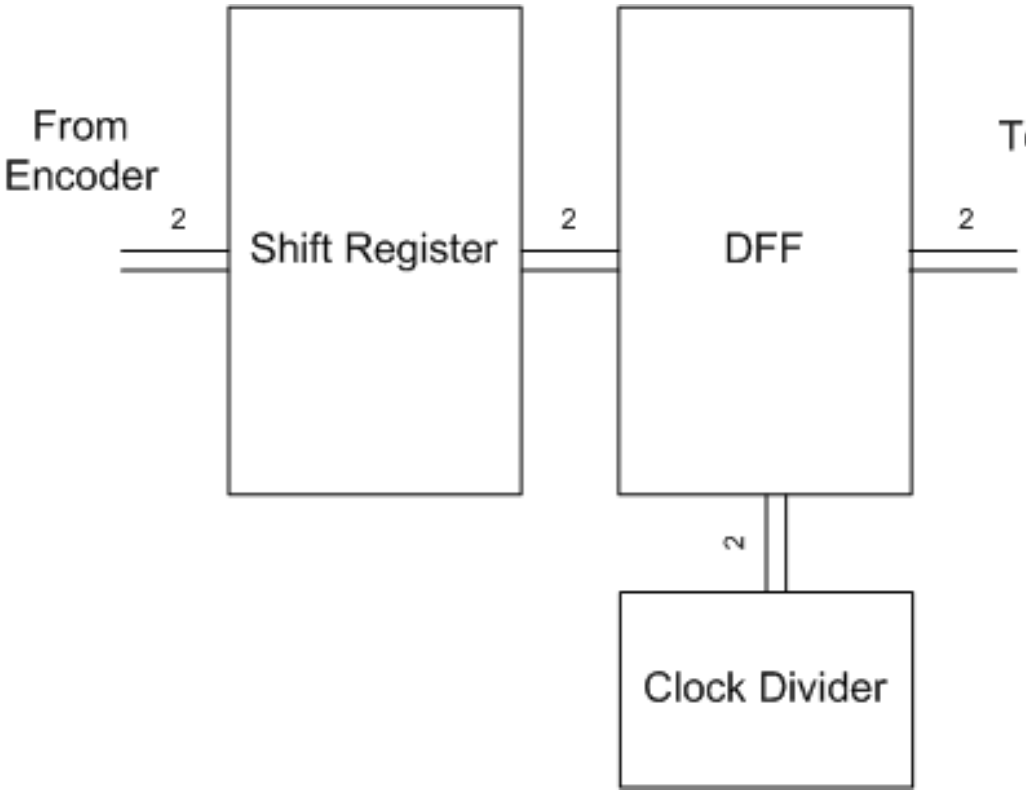
NANDs Outputs



Encoder

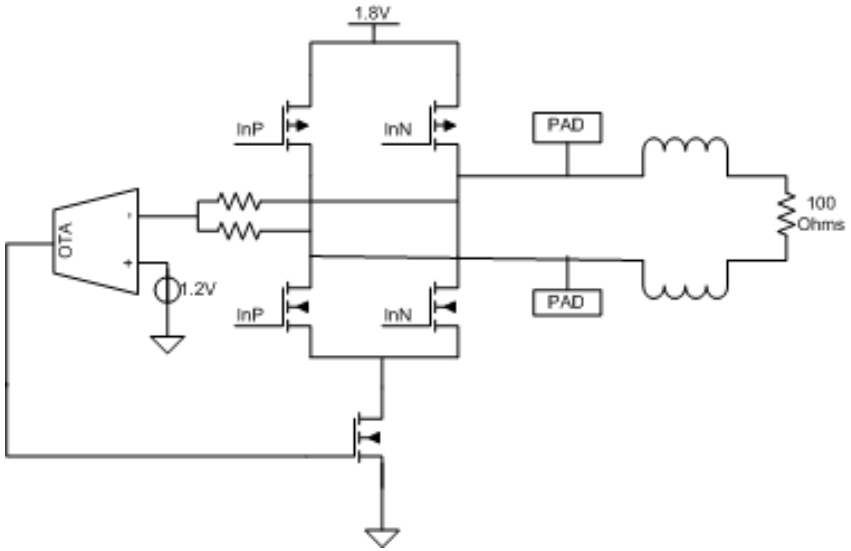

Transient Response
VT("/net0424") - VT("/net0419")
VT("/net0433") - VT("/net0421")
VT("/net0431") - VT("/net0427")
Y0 (V)
Y1 (V)
Y2 (V)
1.5
.5
-.5
-1.5
0 1 2 3 4 5 6 7
0
1
2
3
4
5
6
time (ns)

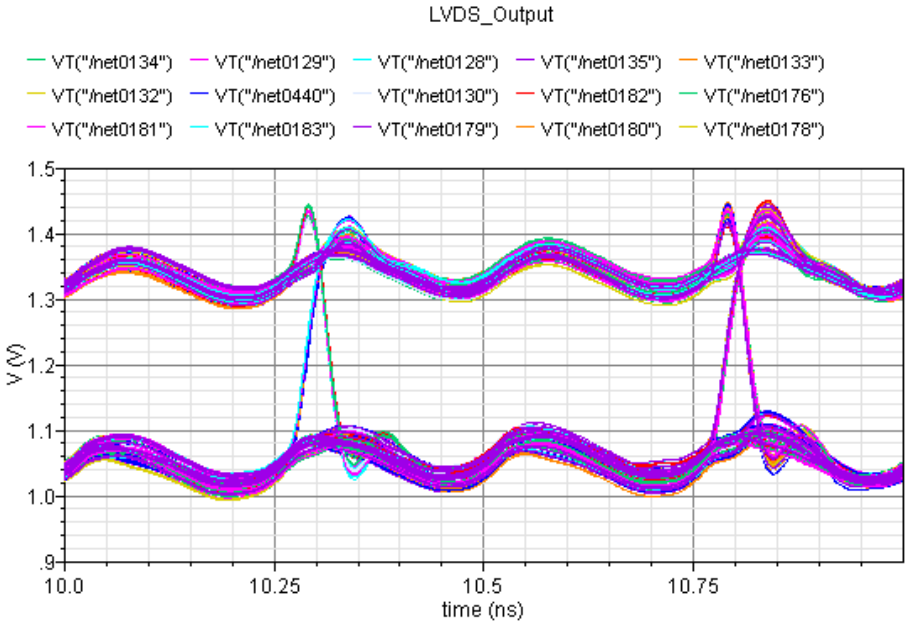
1:4 Demultiplexer



Output Frequency
➔ 2 GHz

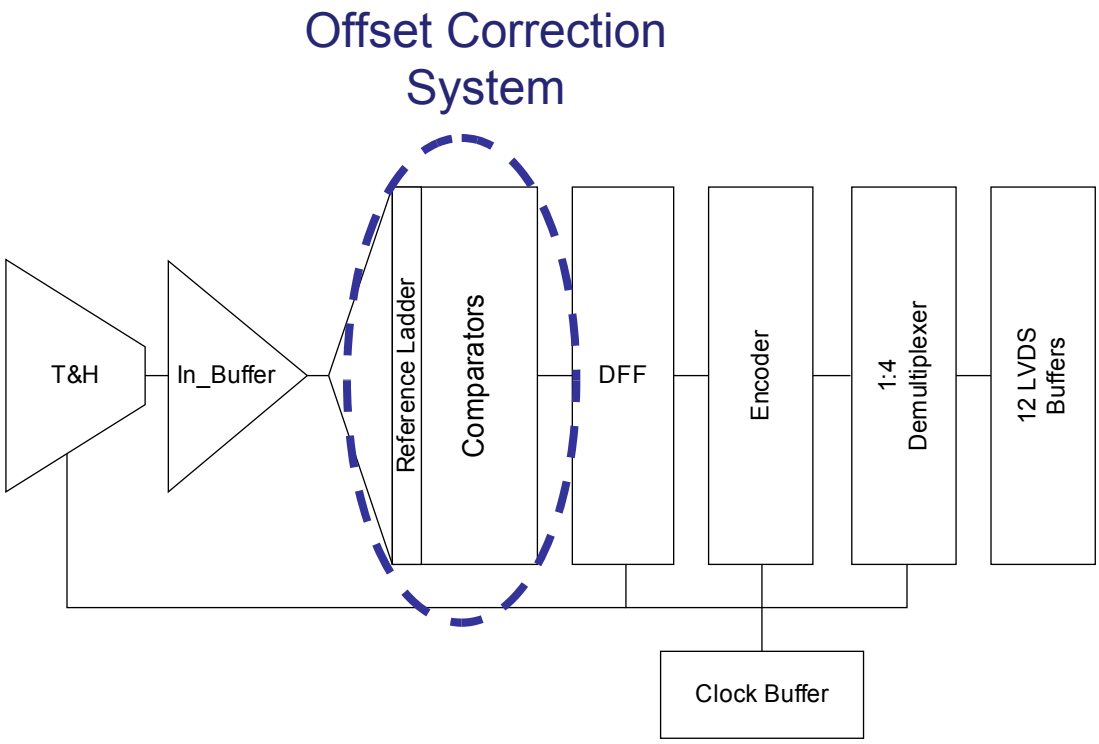
LVDS Buffer


1.8V
InP
InN
PAD
100
Ohms
OTA
1.2V
InP
InN
PAD


LVDS_Output
VT("/net0134")
VT("/net0129")
VT("/net0128")
VT("/net0135")
VT("/net0133")
VT("/net0132")
VT("/net0440")
VT("/net0130")
VT("/net0182")
VT("/net0176")
VT("/net0181")
VT("/net0183")
VT("/net0179")
VT("/net0180")
VT("/net0178")
1.5
1.4
1.3
1.2
1.1
1.0
.9
V (V)
10.0
10.25
10.5
10.75
time (ns)

Conclusion

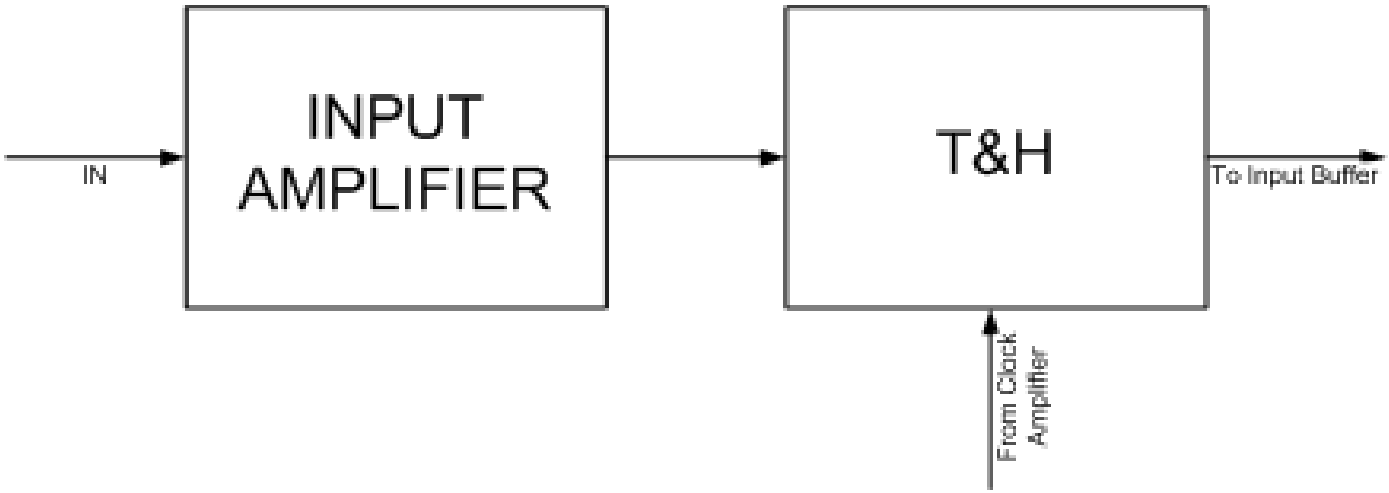
- T&H measurements validate the design methods and the technology models
- 3 bits version design is finished
- Offset correction system in progress
- Layout to be done
- 3 bits version production in November



Overall Power Consumption = 470 mW (401mW+69mW)

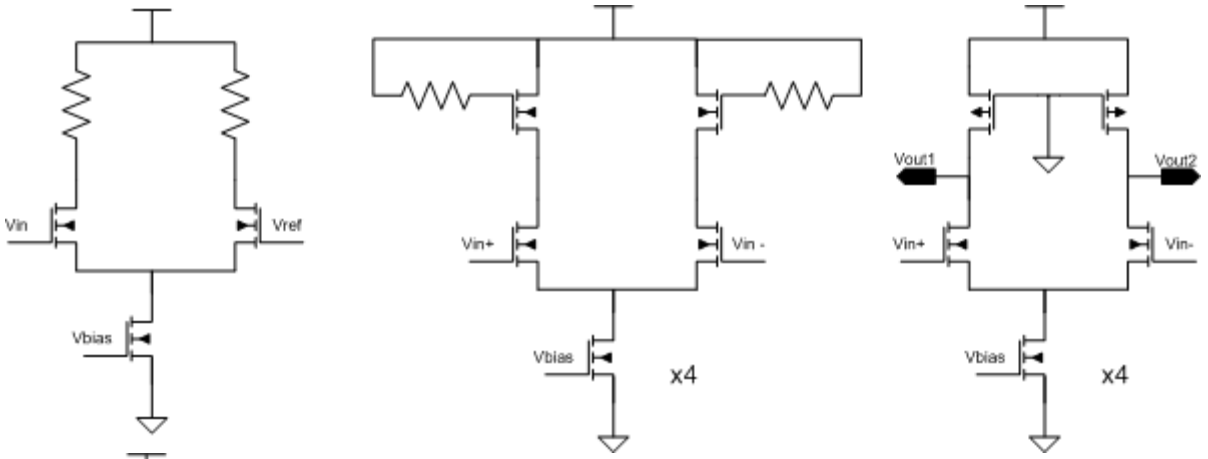
THANK YOU FOR LISTENING

Integrated T&H



Comparators

Single



Differential